
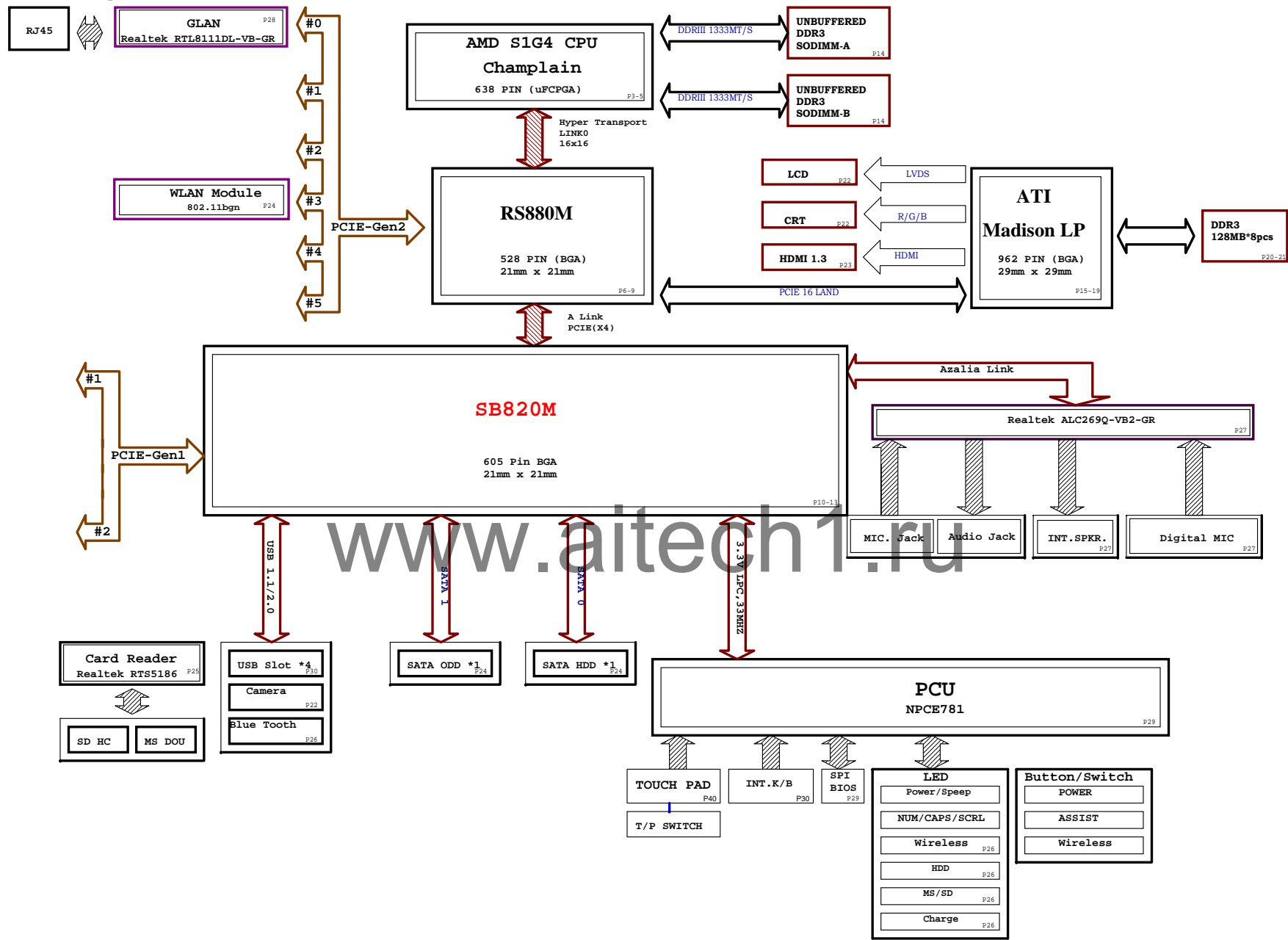


Page	Title of schematic page	Rev.	Date
01	Page List	2A	12/24
02	Block Diagram	2A	12/24
03	CPU-Champlain HT/CONTROL (1/3)	2A	01/04
04	CPU-Champlain MEMORY (2/3)	1B	12/16
05	CPU-Champlain POWER/GND (3/3)	1B	12/08
06	NB-RS880M HT/SP-MEM (1/4)	1B	12/08
07	NB-RS880M GFX/PCIE (2/4)	1A	09/24
08	NB-RS880M SYSTEM (3/4)	1A	09/24
09	NB-RS880M POWER (4/4)	1A	09/24
10	SB-SB820M PCI/CLK/LPC (1/4)	1A	09/24
11	SB-SB820M AUDIO/USB (2/4)	1A	09/24
12	SB-SB820M SATA (3/4)	1B	12/08
13	SB-SB820M POWER (4/4)	1A	09/24
14	DDR3 SODIMM* 2 (5.2mm+9.2mm)	2A	12/24
15	ATI-Madison LP PCIE/LVDS (1/5)	2A	12/24
16	ATI-Madison LP MAIN I/O (2/5)	2A	12/24
17	ATI-Madison LP POWER/GND (3/5)	2A	12/24
18	ATI-Madison LP Display POWER (4/5)	2A	12/24
19	ATI-Madison LP MEM I/F (5/5)	2A	12/24
20	ATI-Madison LP (DDR3 V-ram a)	2A	12/24
21	ATI-Madison LP (DDR3 V-ram b)	1B	12/08
22	CRT/LVDS	2A	12/24

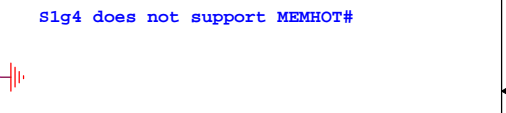
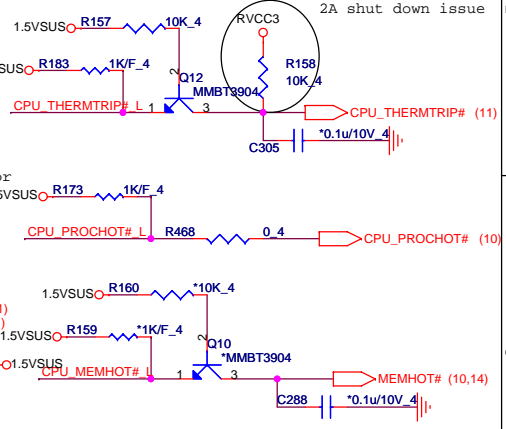
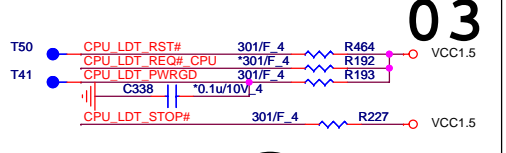
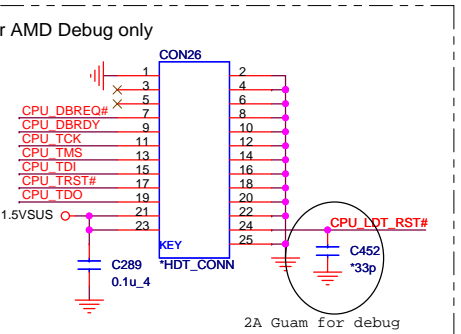
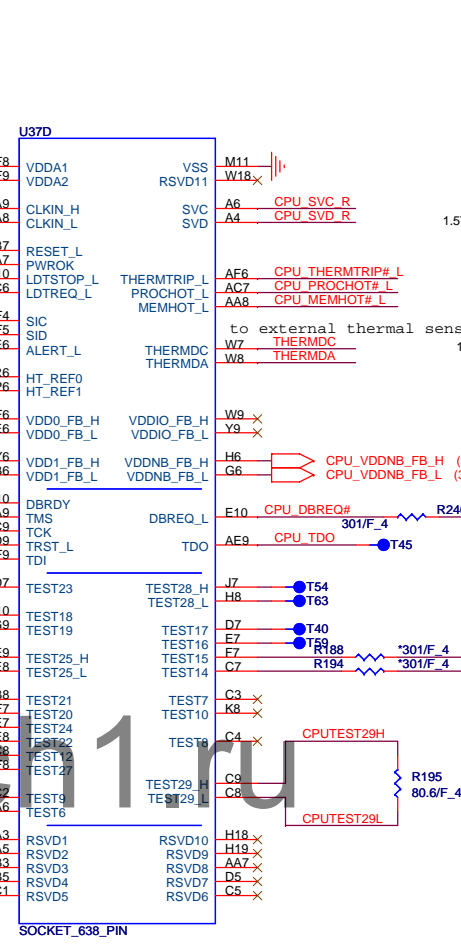
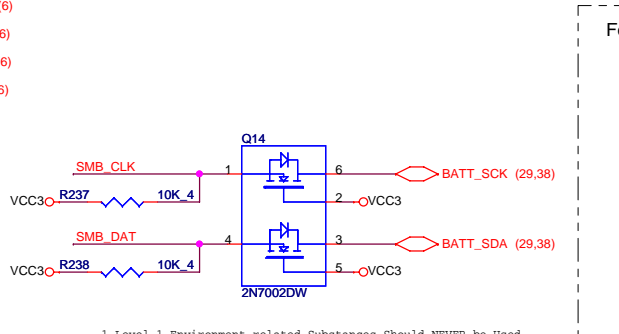
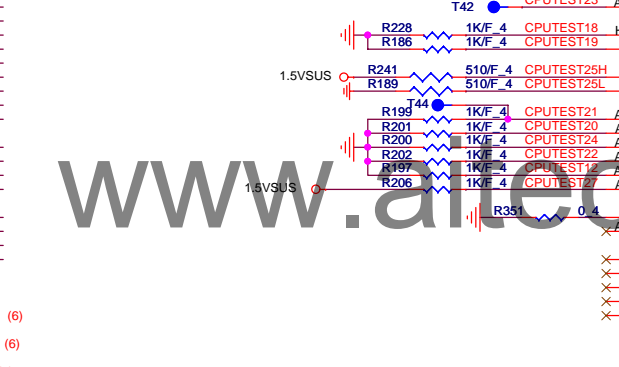
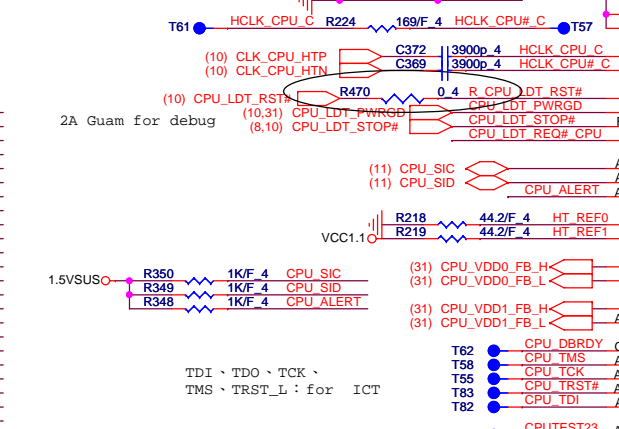
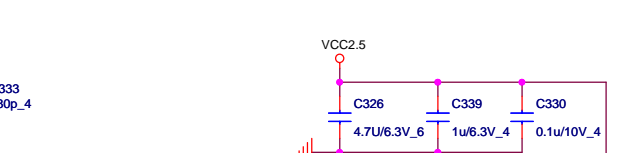
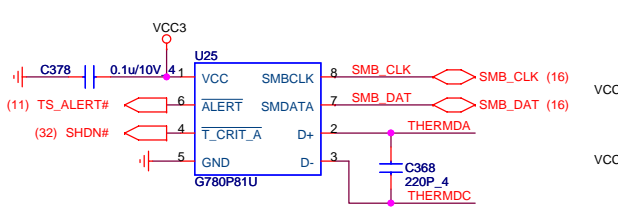
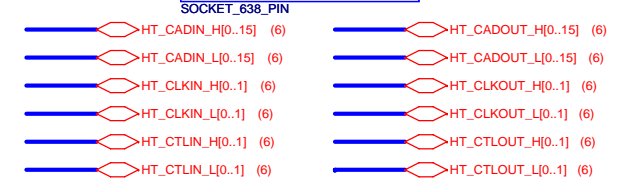
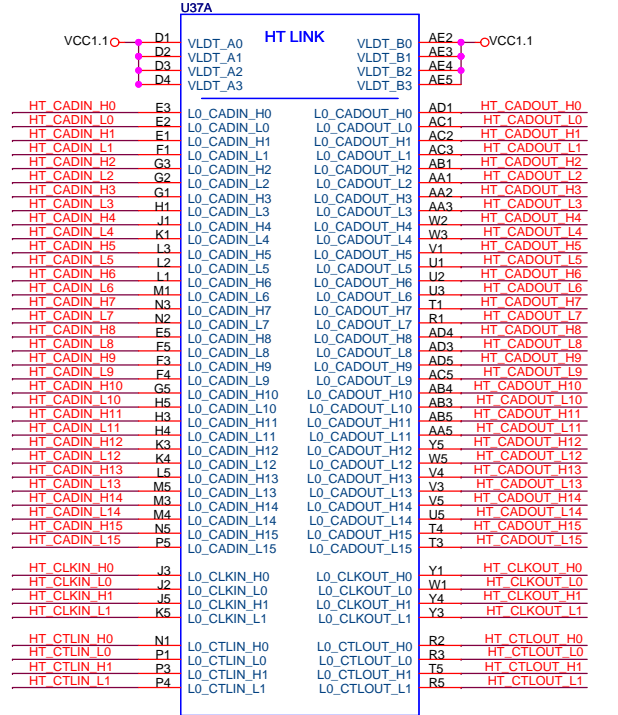
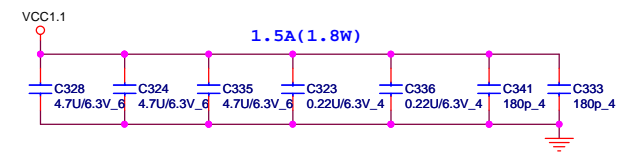
Page	Title of schematic page	Rev.	Date
23	HDMI	1B	12/09
24	WLAN/HDD/ODD	1B	12/08
25	Card Reader RTS5186	1B	12/08
26	Express Card/BT/LED	1B	12/08
27	Codec-ALC269Q VB5 GR	1B	12/08
28	LAN RTL8111E	1B	12/08
29	NPCE781	1B	12/08
30	KB/USB/FAN/PS	1B	12/09
31	VCORE(ISL6265A)	1A	09/24
32	3VPCU&5VPCU(PM6686)	1A	09/24
33	1.5VSUS/VTT_MEM	1A	09/24
34	DYN_VCC1.1(OZ8116LN)	1A	09/24
35	VCC1.1(OZ8116LN)-7A	1A	09/24
36	VGA_CORE(OZ8116)-16A	1A	09/24
37	VCC1.8/0.9/2.5/1.0	1A	09/24
38	POWER(BAT IN / ADA IN/ UL)	1A	09/24
39	CHARGER (ISL6252A)	1A	09/24
40	Small board connector	1A	09/24
41	Power Sequence		
42	CHANGE LIST		

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

 Quanta Computer Inc. PROJECT : NE8		Rev 2A
AMD Danube		
Date:	Wednesday, January 27, 2010	Sheet 1 of 42

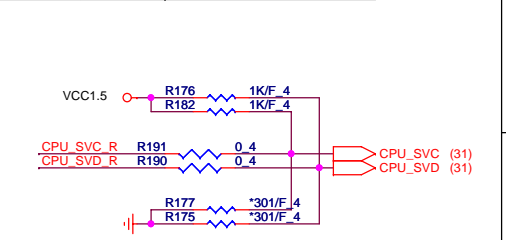


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VFIX MODE VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



Quanta Computer Inc.
PROJECT : NE8

Size: Document Number: CPU HT/CONTROL(1/3) Rev: 2A

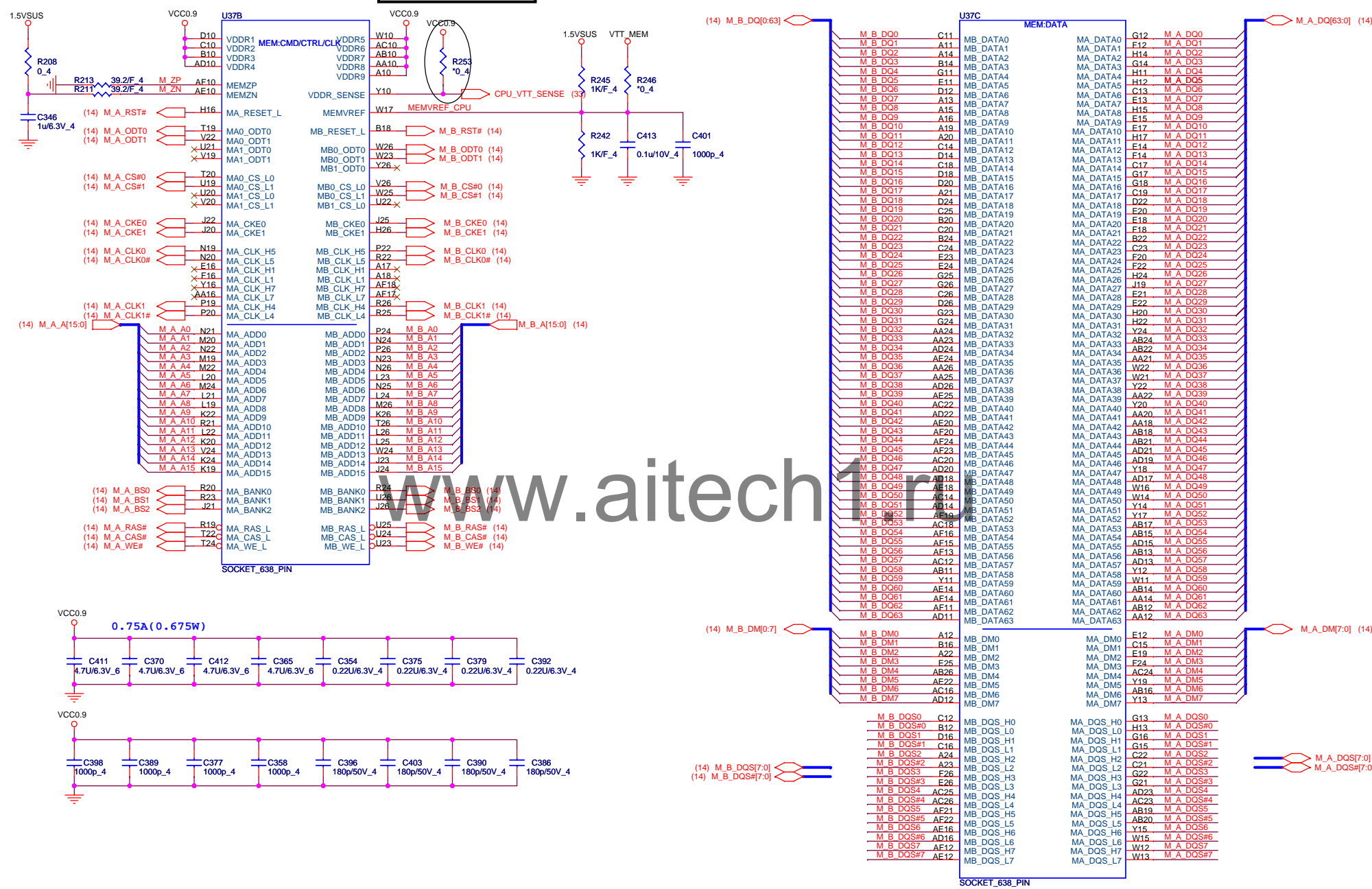
Date: Wednesday, January 27, 2010 Sheet: 3 of 42

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1.Level 1 Environment-related Substances Should NEVER be Used.
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Processor Memory Interface

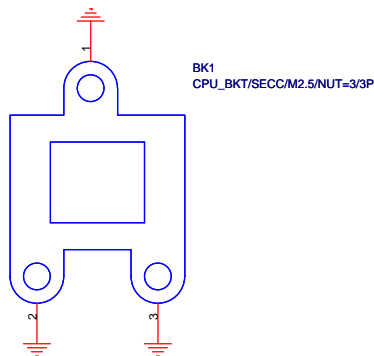
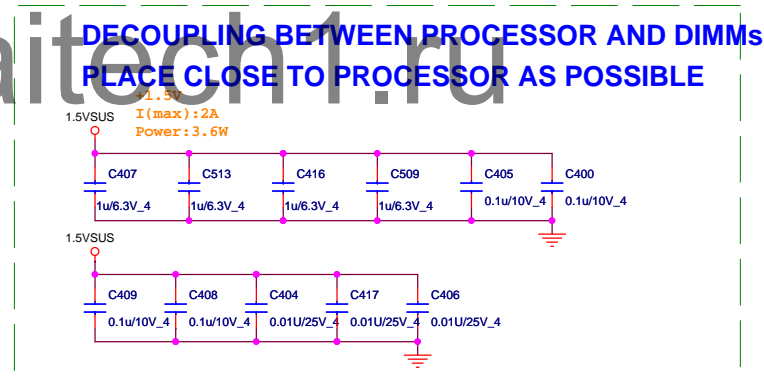
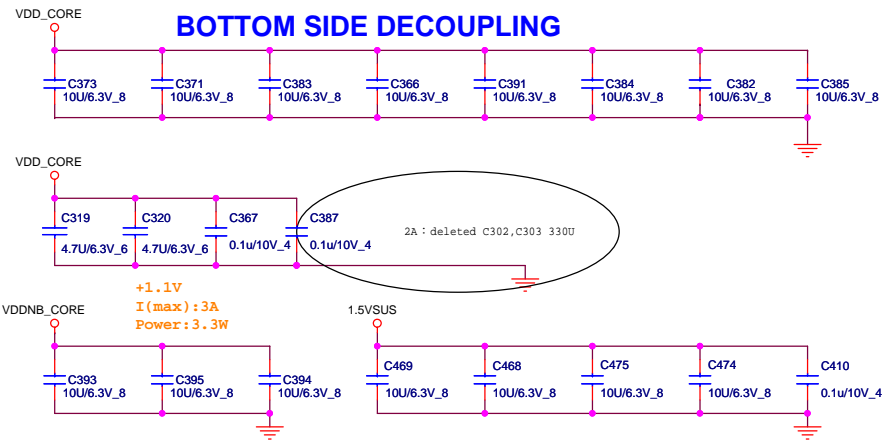
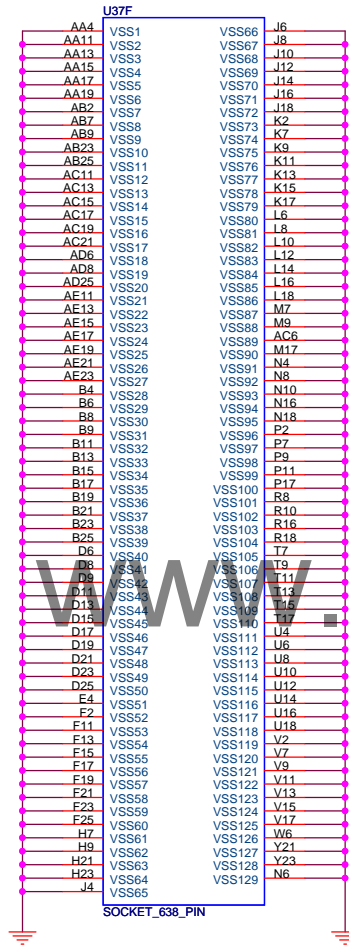
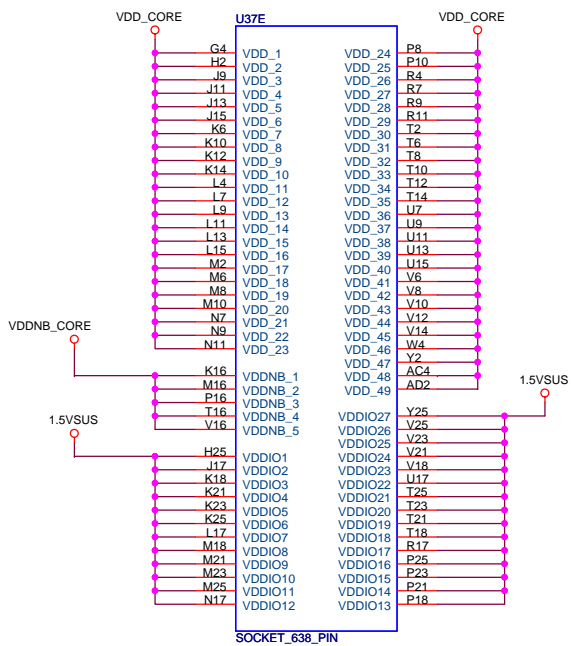
CPU_VDDR : 35W->0.9V
45W->1.05V



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Socket Type	QCI P/N
Normal	DG0^8000018
90 degree	DG0^8000023

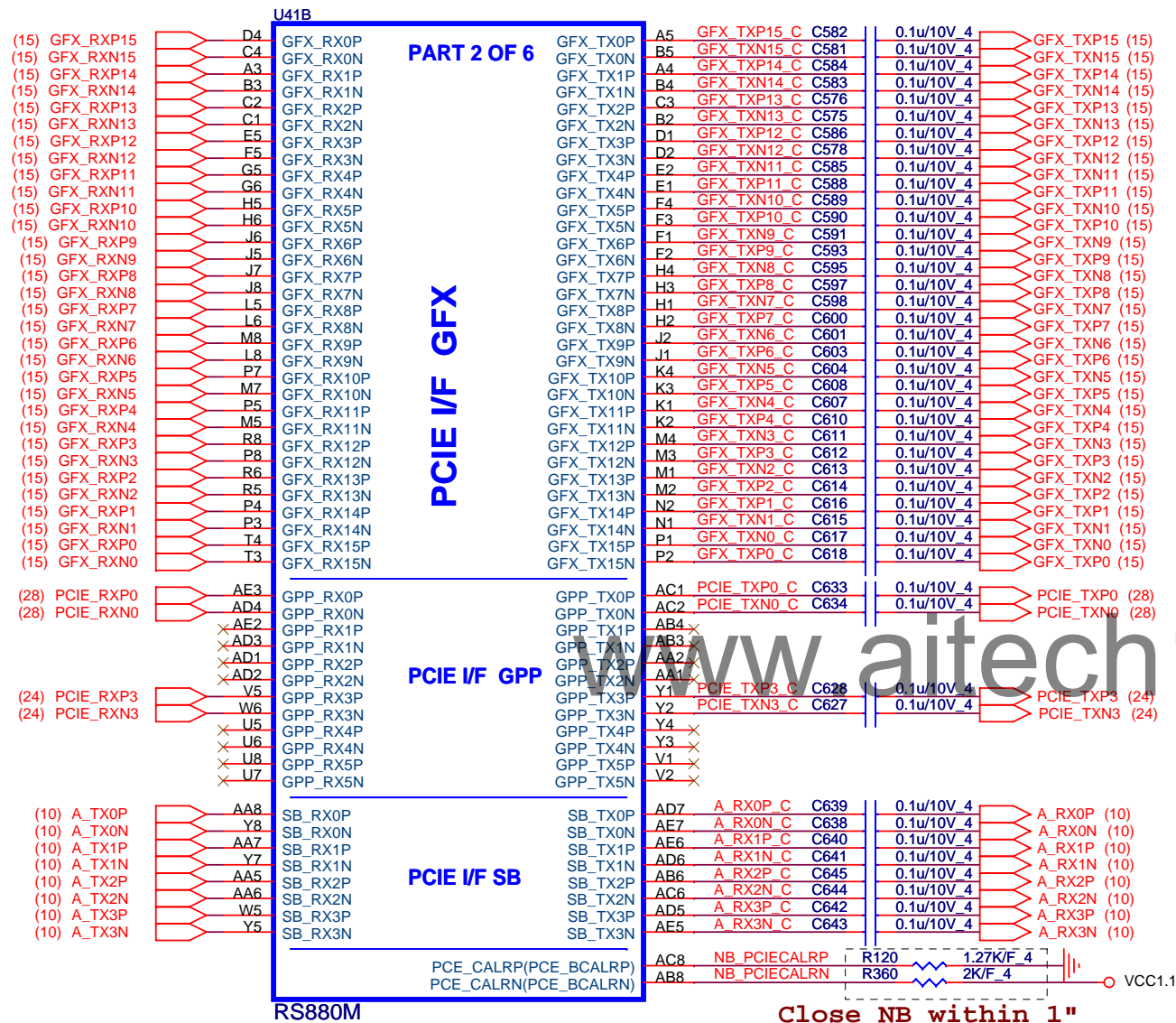




HYPER TRANSPORT CPU I/F

This block is for Side Port only, others can remove some components





Layout Swap
 TX11, TX10, TX9,
 TX8, TX7, TX6, TX5,
 TX4, TX3, TX2, TX0

GLAN

WLAN

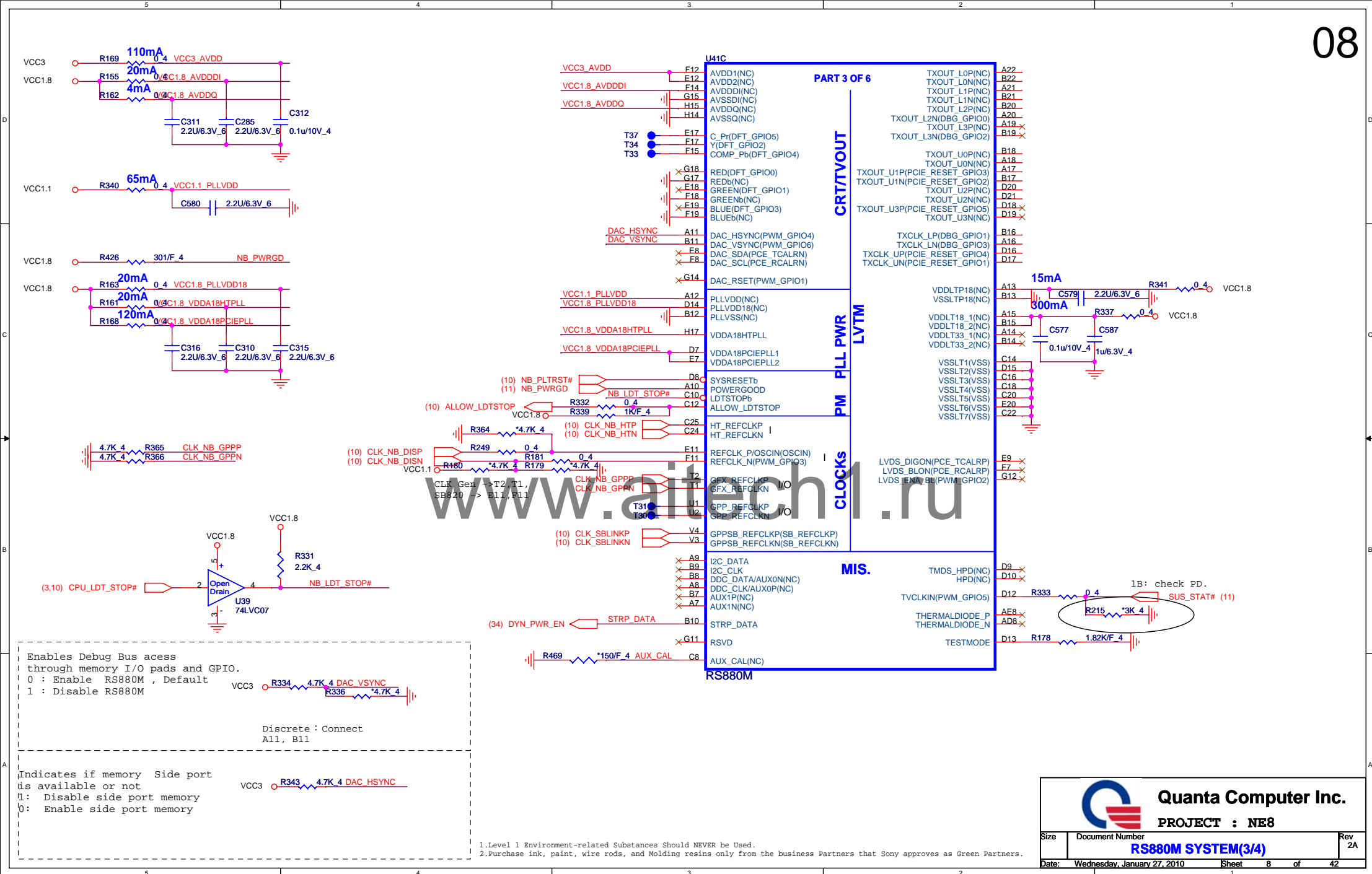


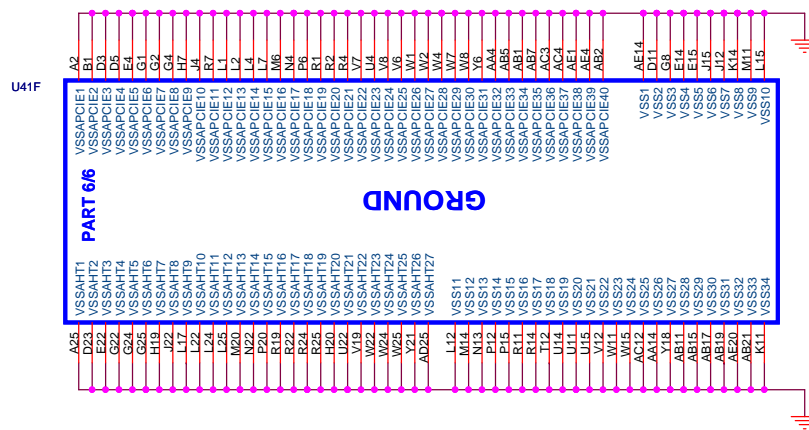
Quanta Computer Inc.

PROJECT : NE8

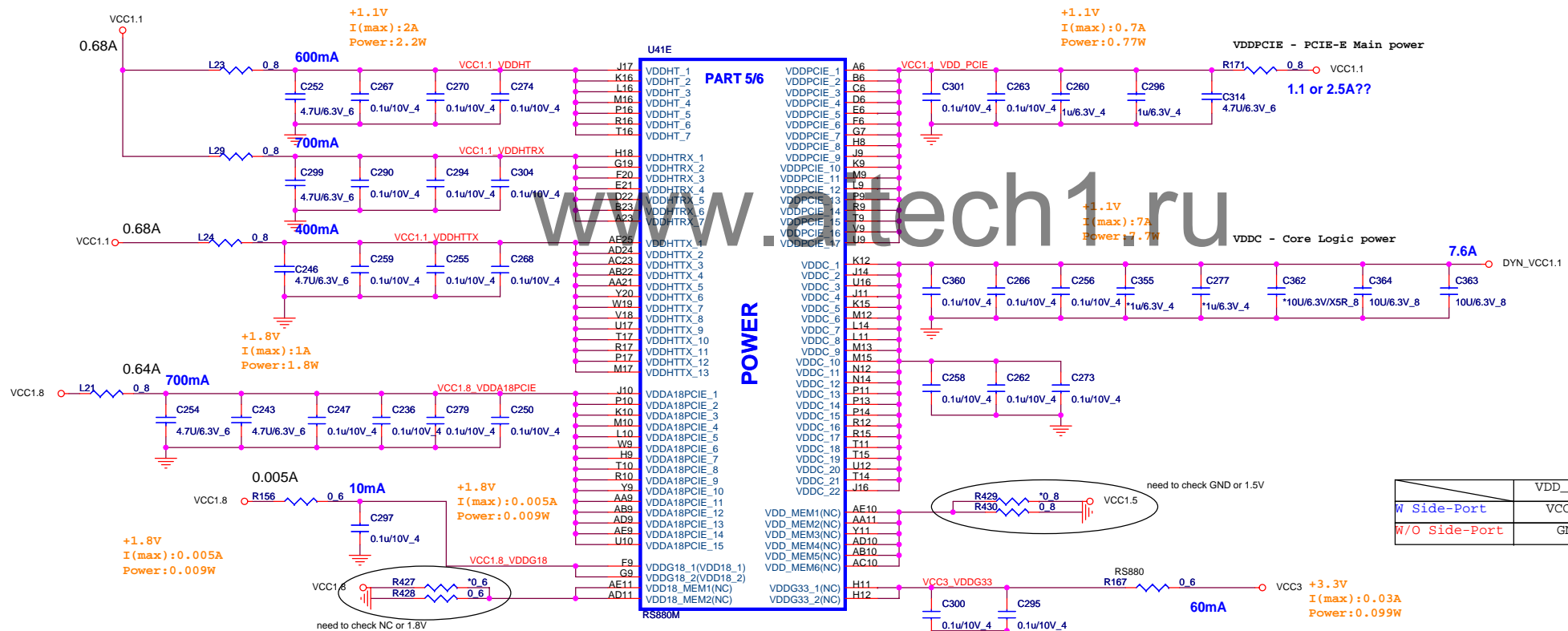
Size	Document Number	Rev
	RS880M GFX/PCIE(2/4)	2A
Date:	Wednesday, January 27, 2010	Sheet 7 of 42

- 1.Level 1 Environment-related Substances Should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.





RS880M/RX881 POWER DIFFERENCE TABLE					
PIN NAME	RX881	RS880M	PIN NAME	RX881	RS880M
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.1V	+1.1V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLTP18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDLTP33	NC	NC




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	VDD18_MEM
W Side-Port	VCC1.8
W/O Side-Port	GND

	VDD_MEM
W Side-Port	VCC1.5
W/O Side-Port	GND

VDD18_MEM For UMA RS880 only
Not applicable to RX881
memory I/O transform



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Size	Document Number	Rev
		2A
RS880M POWER(4/4)		
Date	Wednesday, January 27, 2010	Sheet 9 of 42

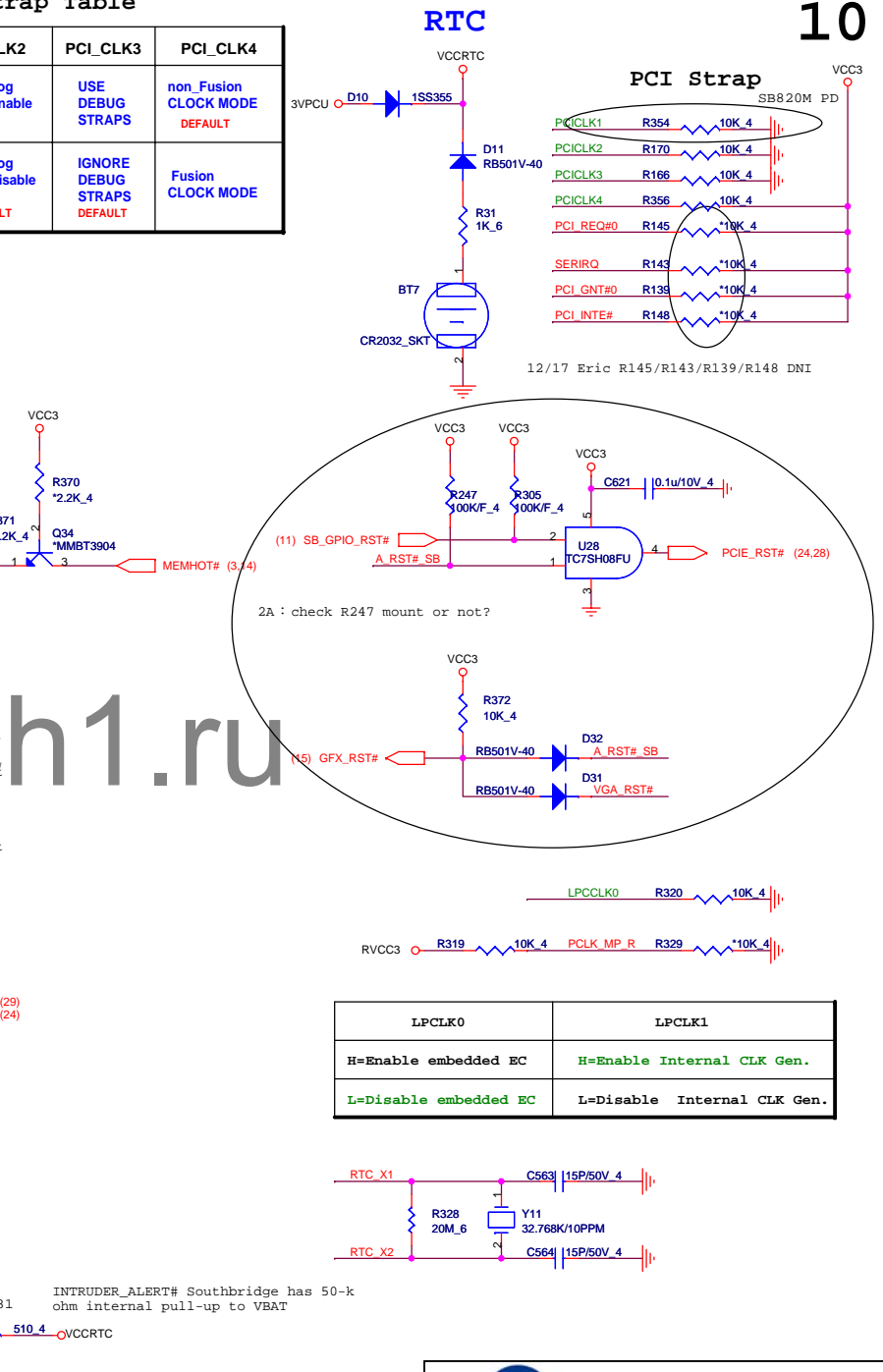
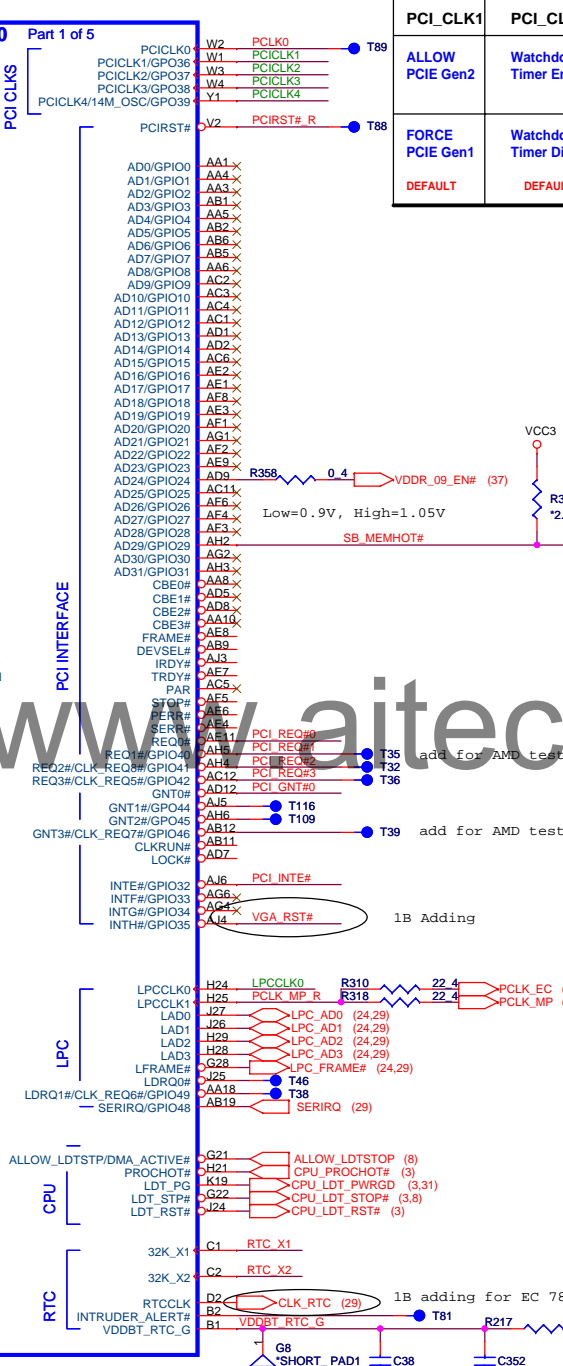
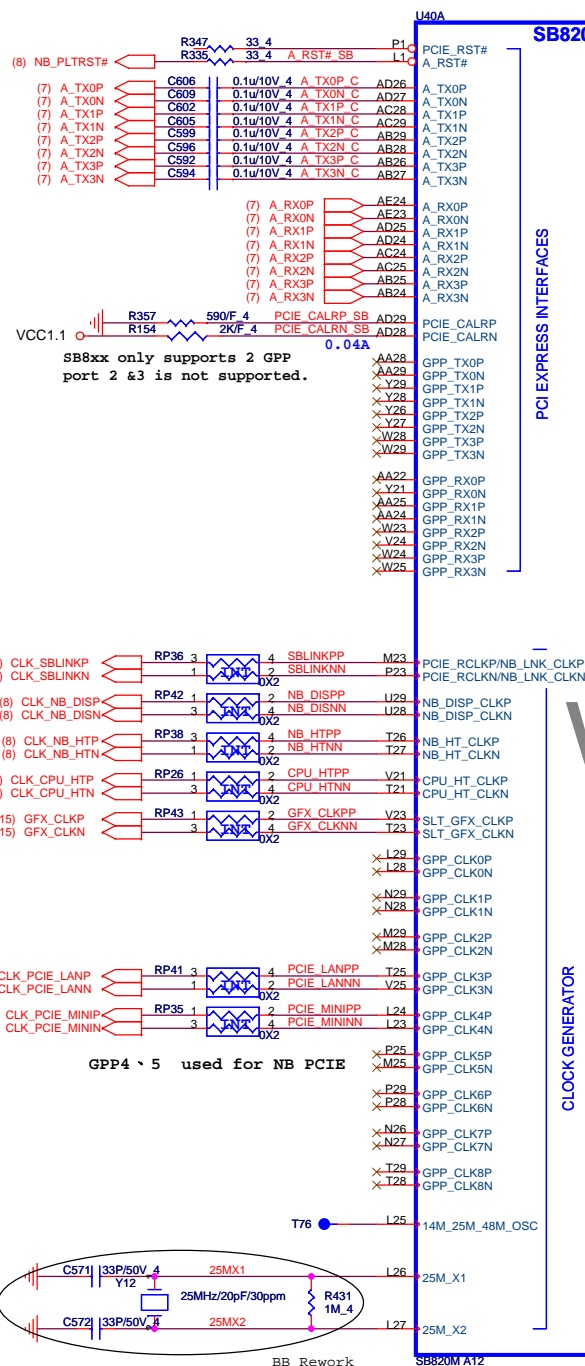
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Strap Table

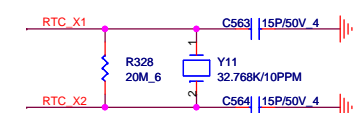
PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4
ALLOW PCIe Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT
FORCE PCIe Gen1	Watchdog Timer Disable	IGNORE DEBUG STRAPS	Fusion CLOCK MODE
DEFAULT	DEFAULT	DEFAULT	

RTC

10



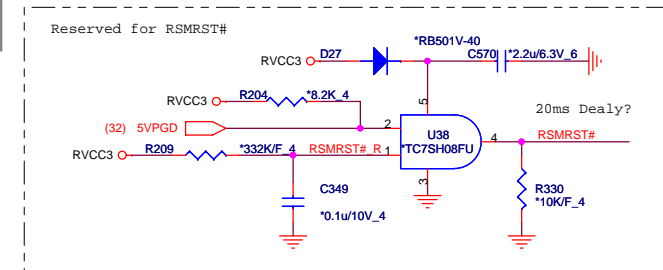
LPCLK0	LPCLK1
H=Enable embedded EC	H=Enable Internal CLK Gen.
L=Disable embedded EC	L=Disable Internal CLK Gen.



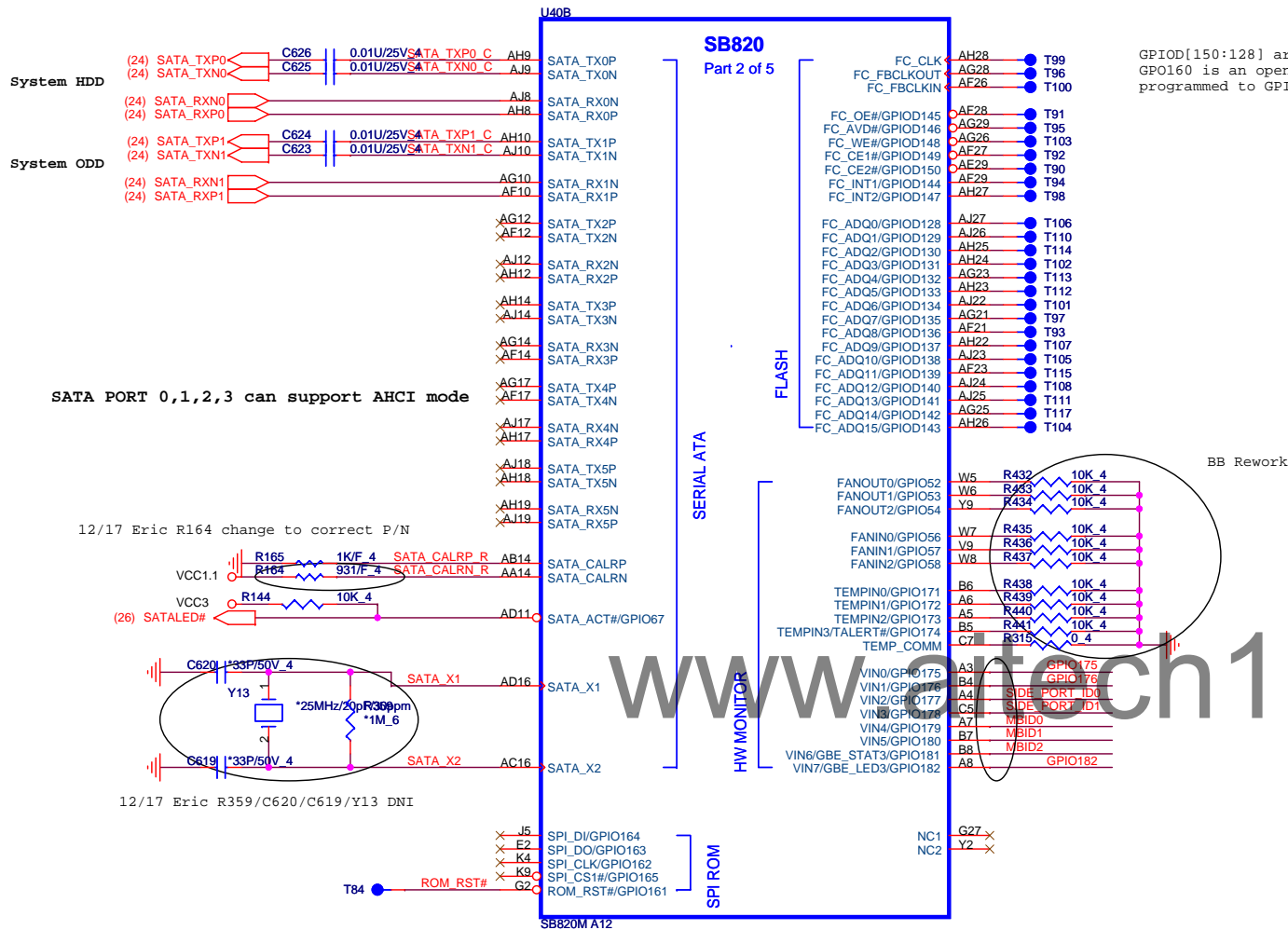
Quanta Computer Inc.
PROJECT : NE8

Size	Document Number	Rev
	SB820M PCI/CLK/LPC(1/4)	2A
Date:	Thursday, January 28, 2010	Sheet 10 of 42

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



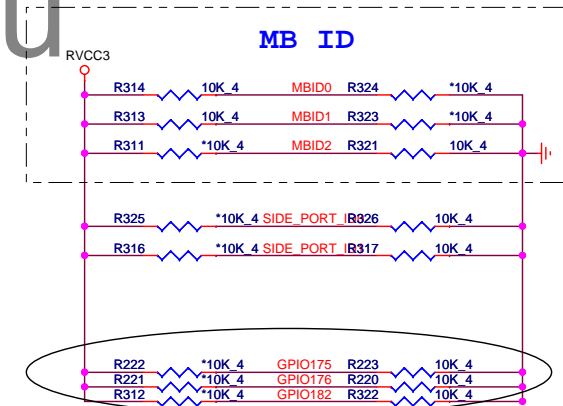
	GPIO200, GPIO199
PULL HIGH	H, H=Reserved H, L=SPI ROM
PULL LOW	L, H=LPC ROM(Default) L, L=FWH ROM




GPIO[150:128] are open drain GPIO pins where as GP0160 is an open drain GPO pin. These pins are not programmed to GPIO mode by default.

ID2	ID1	ID0	
0	0	0	Danube UMA
0	0	1	Danube UMA+Side port
0	1	0	Danube+Park XT
0	1	1	Danube+Madison LP
1	0	0	Danube+M92 XTX
1	0	1	
1	1	0	
1	1	1	

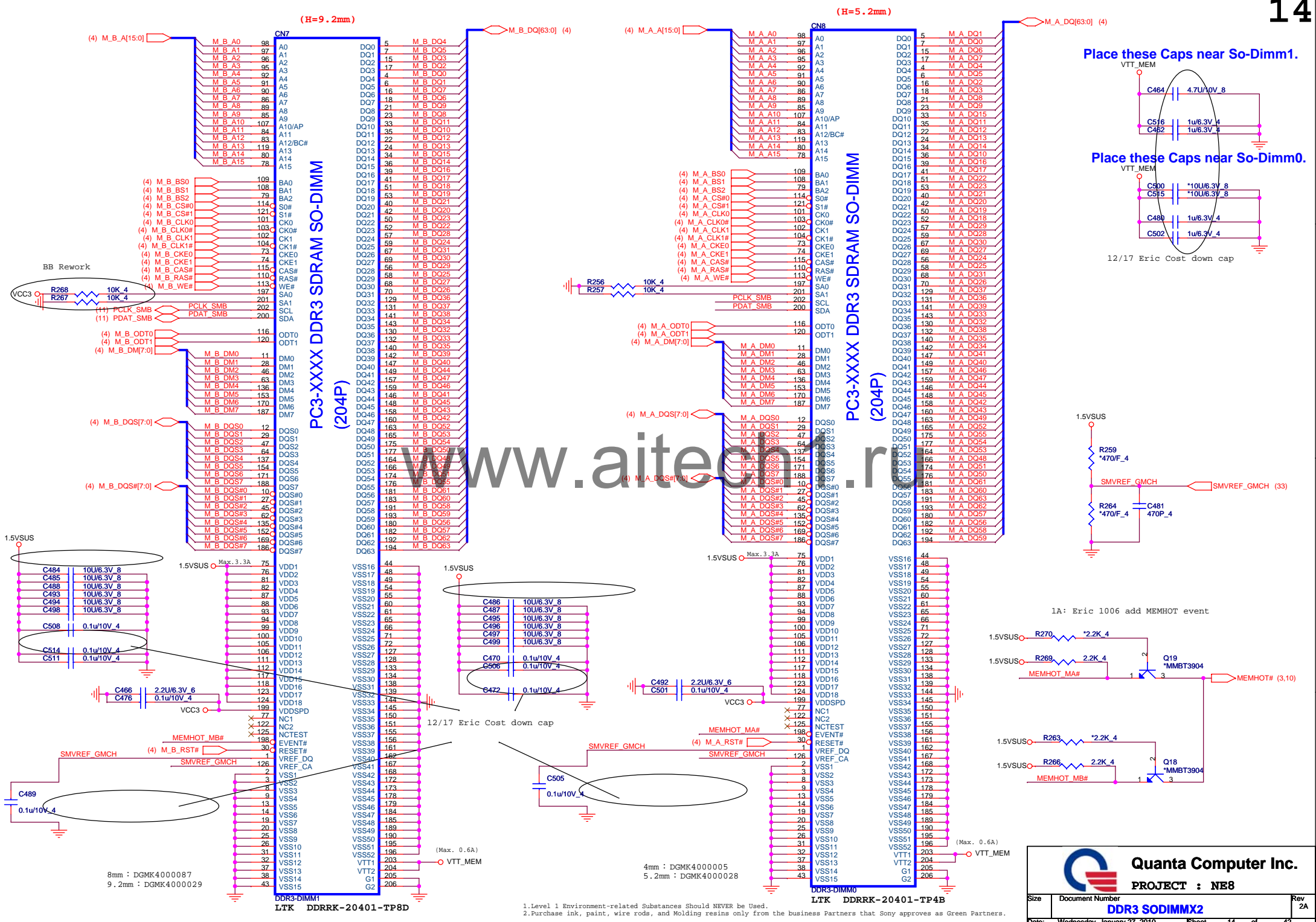
	NON	SAMSUNG	HYNIX	
SP ID0	0	1	0	1
SP ID1	0	0	1	1



- 1.Level 1 Environment-related Substances Should NEVER be Used.
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 Quanta Computer Inc. PROJECT : NE8		Size	Document Number	Rev
			SB820 SATA(2/4)	2A
Date:	Wednesday, January 27, 2010	Sheet	12	of 42

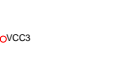
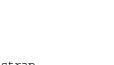
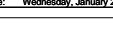
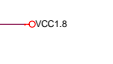
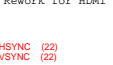
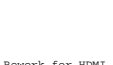
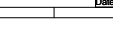
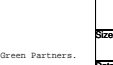
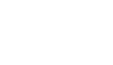
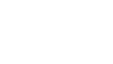
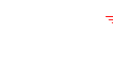
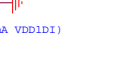
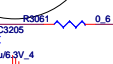
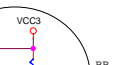
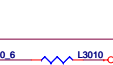
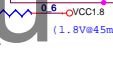
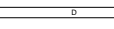
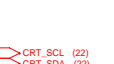
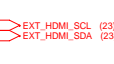
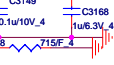
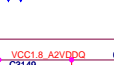
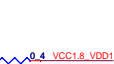
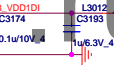
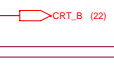
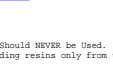
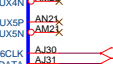
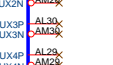
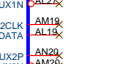
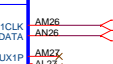
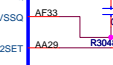
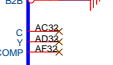
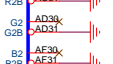
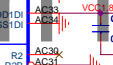
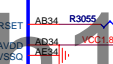
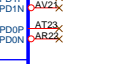
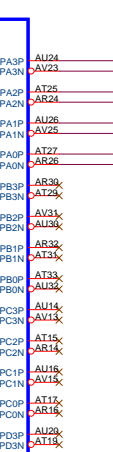
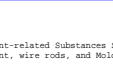
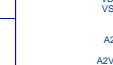
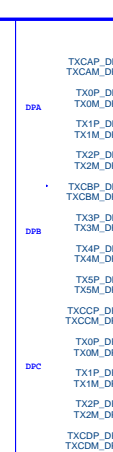
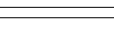
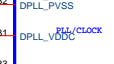
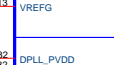
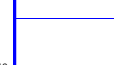
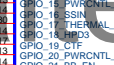
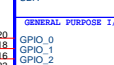
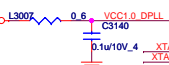
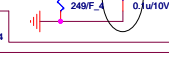
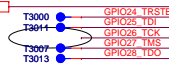
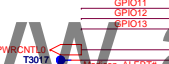
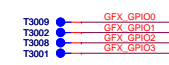
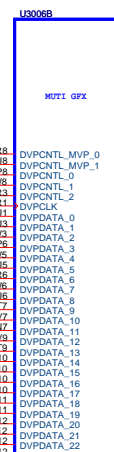
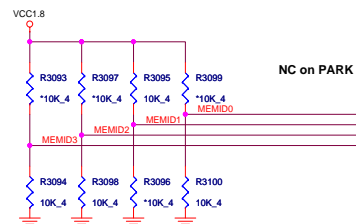


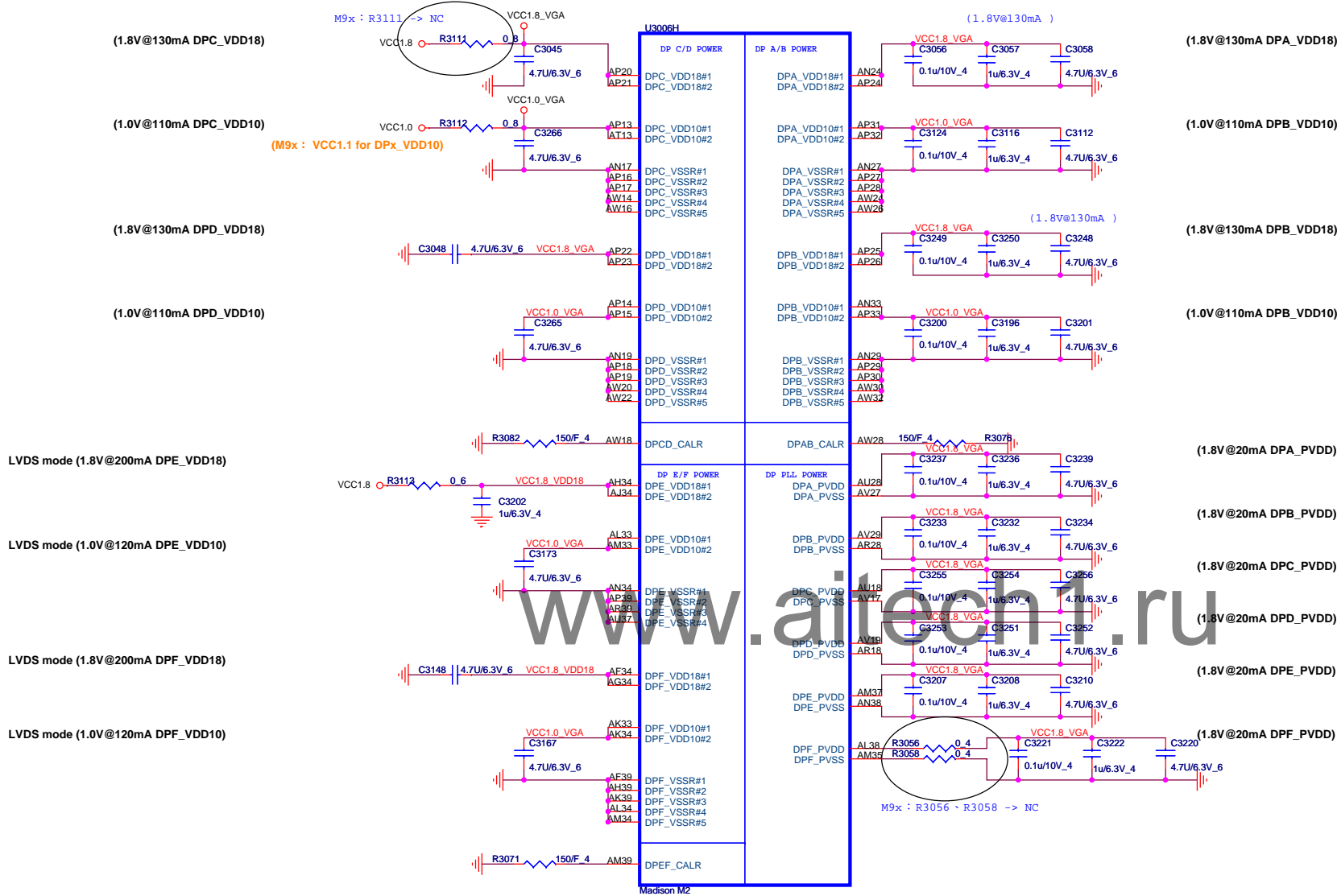


MEMID[3:0]	Vendor	Type	Vendor P/N
0000			
0001	Hynix	64*16-800MHZ	H5TQ1G63BFR-12C
0010	Samsung	64*16-800MHZ	K4W1G1646E-HC12
0011	Ati	64*16-800MHZ	23EY2387MA-12
0100		Reserved	
0101		Reserved	
0110		Reserved	
0111		Reserved	
1000		Reserved	
1001		Reserved	
1010		Reserved	
1011		Reserved	
1100		Reserved	
1101		Reserved	
1110		Reserved	
1111		Reserved	

Samsung 64*16-900MHZ K4W1G1646E-HC11


AKD5LZGTW00
AKD5LZGT502
AKD5LZGT701



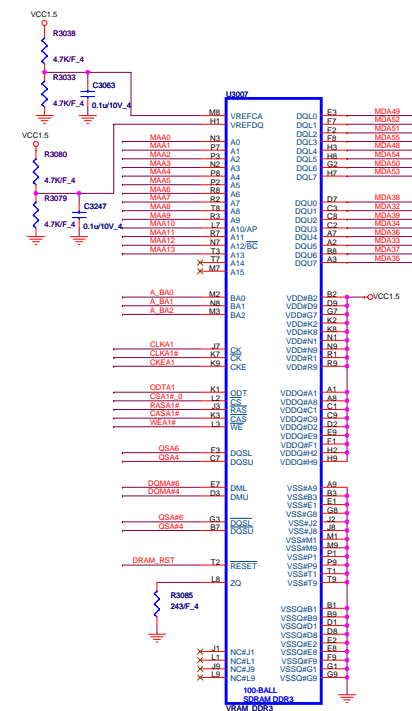
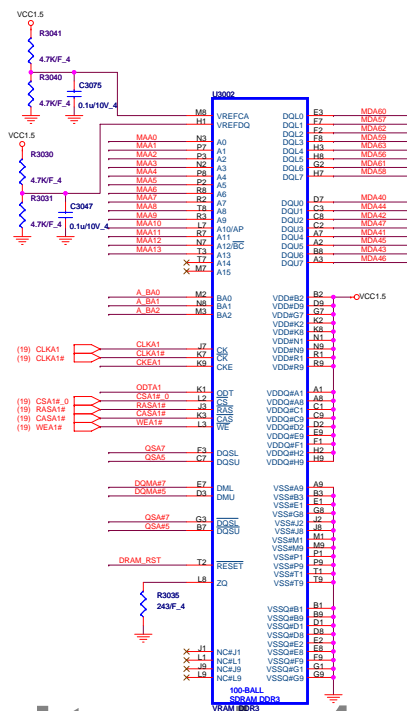
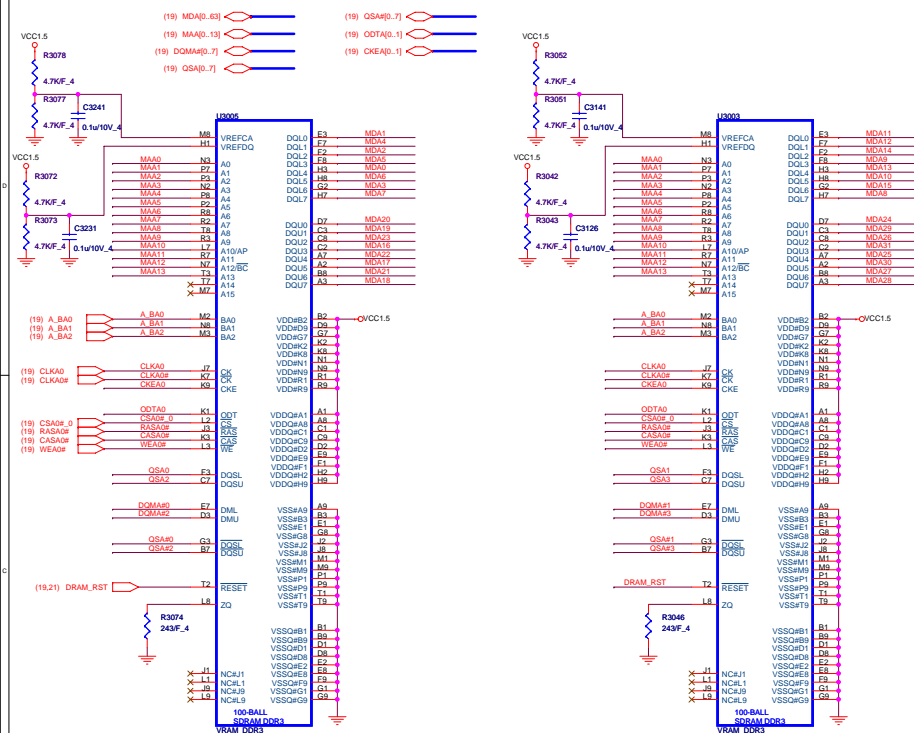


1.Level 1 Environment-related Substances Should NEVER be Used.
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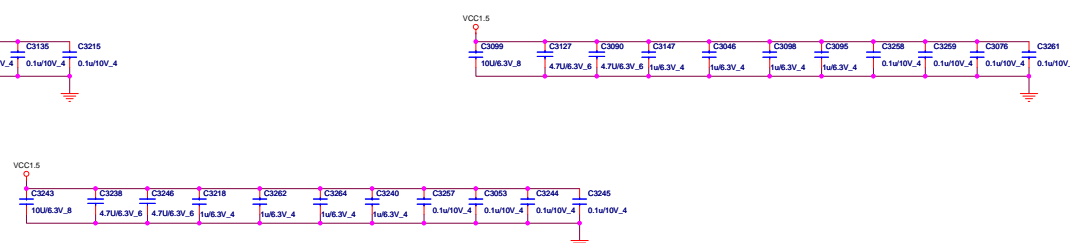
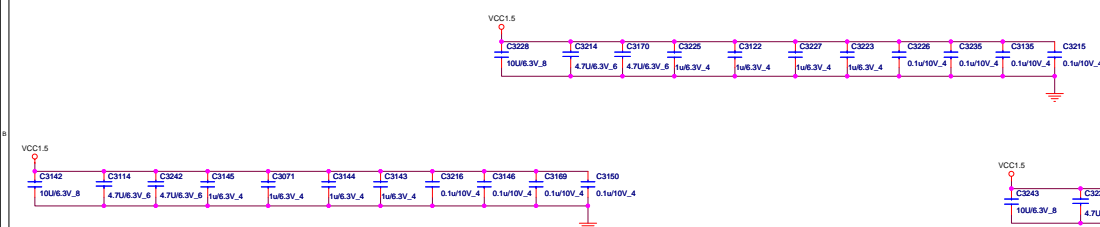
Use this option ONLY
for Park-S3

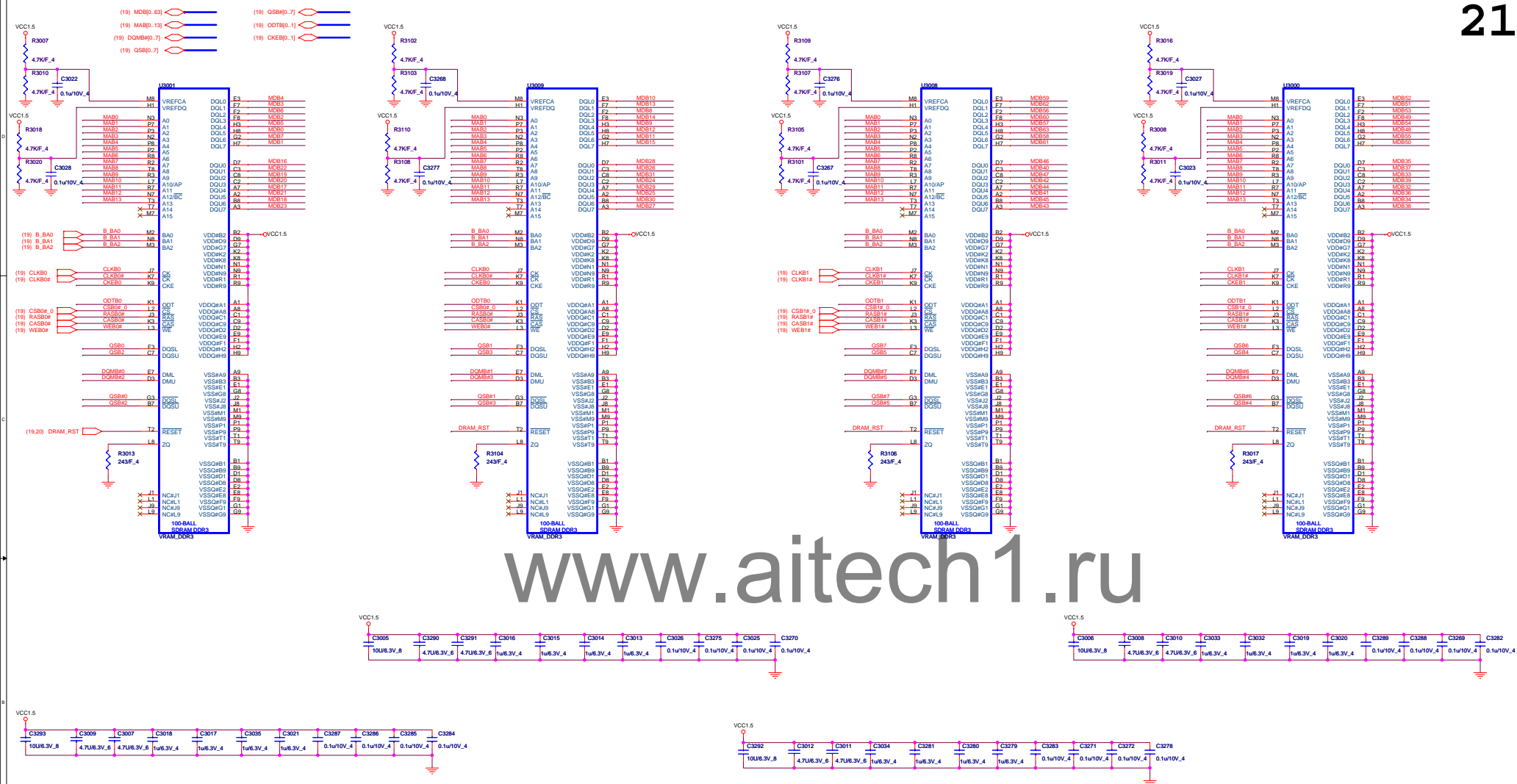
 Quanta Computer Inc. PROJECT : NE8		
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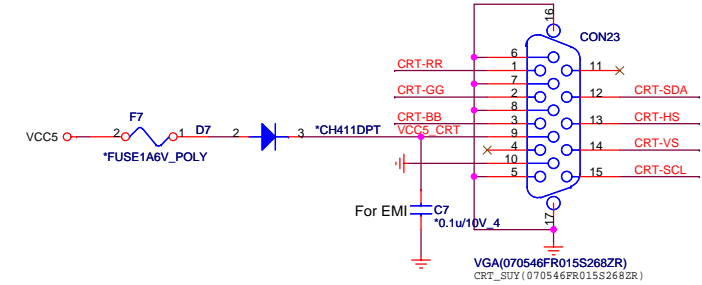
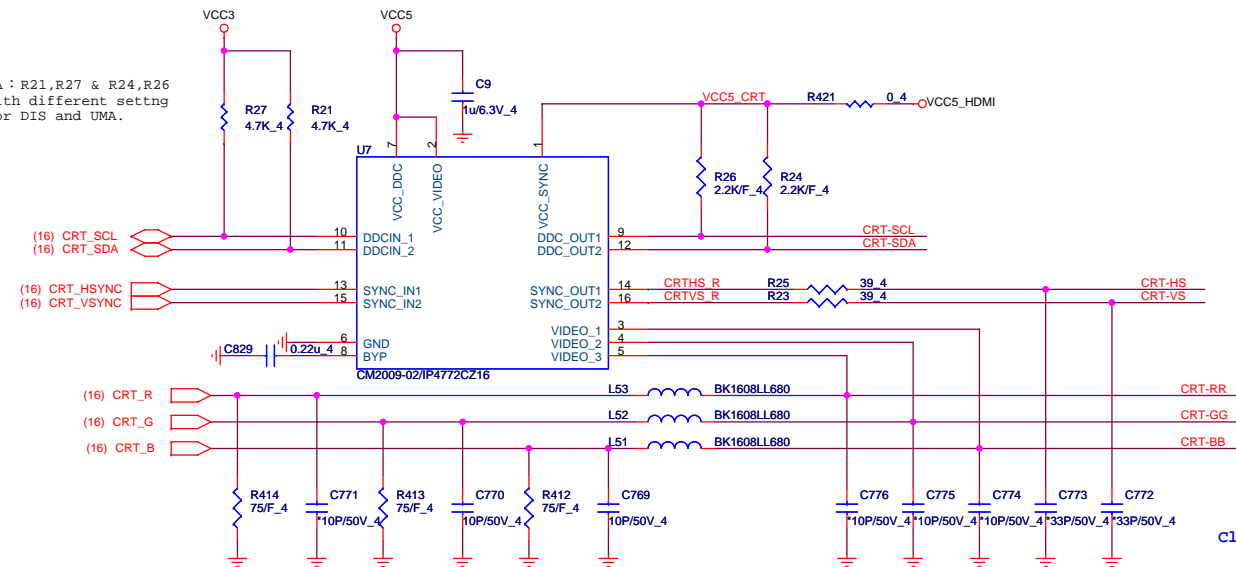




CRT

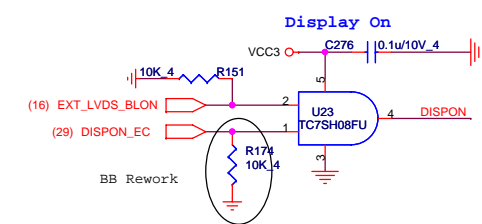
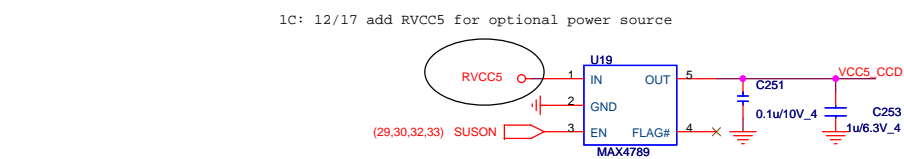
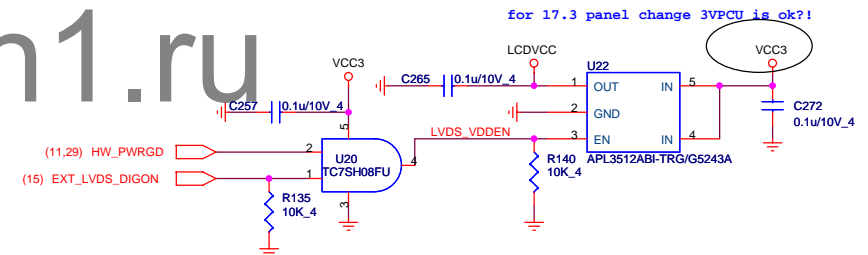
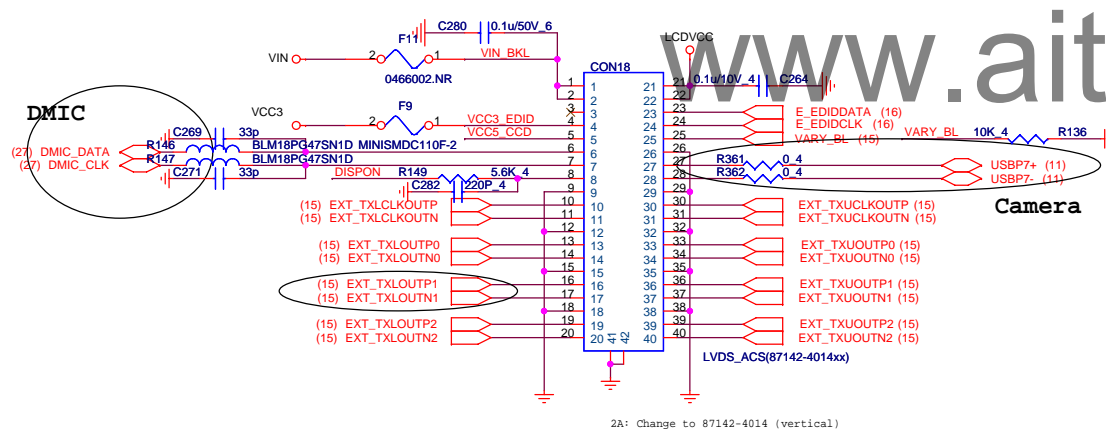
22

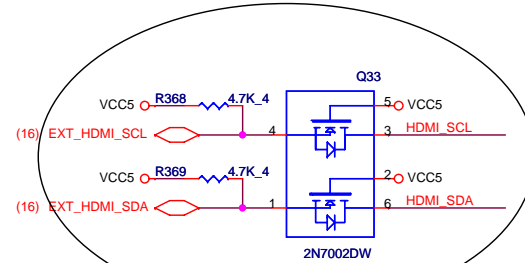
2A: R21, R27 & R24, R26 with different setting for DIS and UMA.



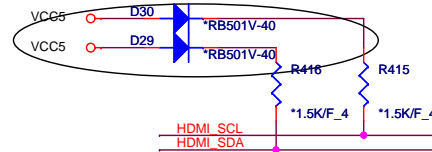
Close to Con3

LVDS

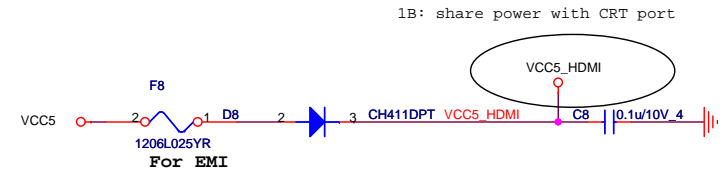
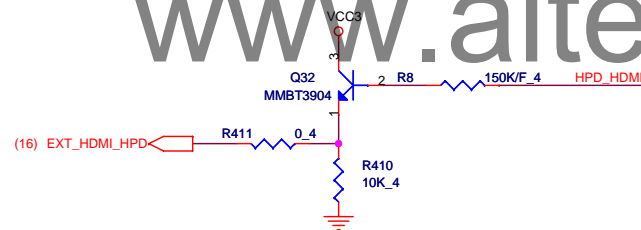




1B: add diode for HDMI test



12/17 Eric D29/D30/R416/R415 DNI

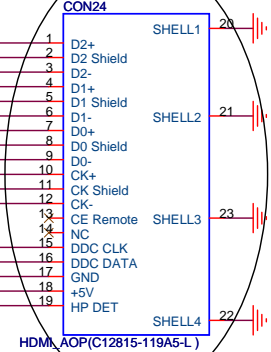


EXT HDMI TXDP0 R420 *100/F 4 EXT HDMI TXDN0
EXT HDMI TXDP1 R418 *100/F 4 EXT HDMI TXDN1
EXT HDMI TXDP2 R419 *100/F 4 EXT HDMI TXDN2
HDMI TXCP R417 *100/F 4 HDMI TXCN

(16) EXT_HDMI_TXCP 3 4 HDMI TXCP
(16) EXT_HDMI_TXCN 1 2 HDMI TXCN

ATI Suggestion close to Con24

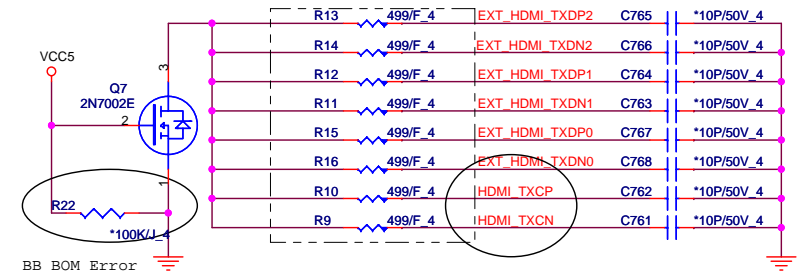
(16) EXT_HDMI_TXDP2 C675 0.1u/10V 4 EXT HDMI TXDP2 C
(16) EXT_HDMI_TXDN2 C676 0.1u/10V 4 EXT HDMI TXDN2 C
(16) EXT_HDMI_TXDP1 C677 0.1u/10V 4 EXT HDMI TXDP1 C
(16) EXT_HDMI_TXDN1 C678 0.1u/10V 4 EXT HDMI TXDN1 C
(16) EXT_HDMI_TXDP0 C679 0.1u/10V 4 EXT HDMI TXDP0 C
(16) EXT_HDMI_TXDN0 C680 0.1u/10V 4 EXT HDMI TXDN0 C
HDMI TXCP C681 0.1u/10V 4 EXT HDMI TXCP C
HDMI TXCN C688 0.1u/10V 4 EXT HDMI TXCN C



0115 change connector, need update P/N

ATI Suggestion close to Con24

For ESD



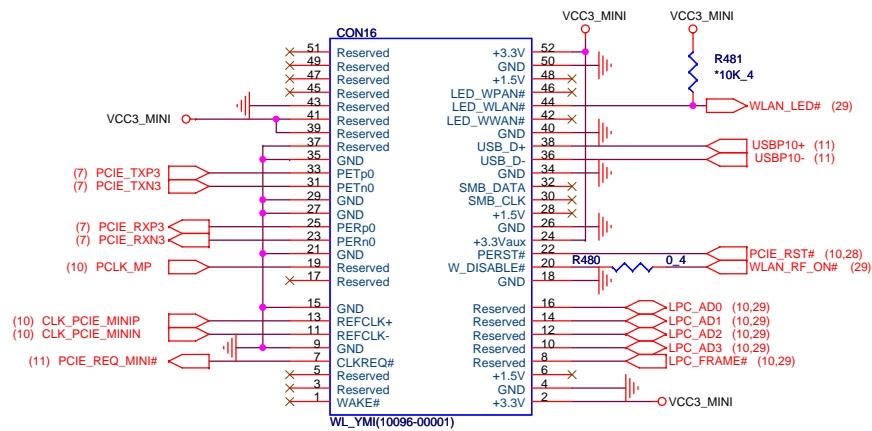
BB BOM Error
100K ohm
12/17 Eric R22 DNI



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HDMI
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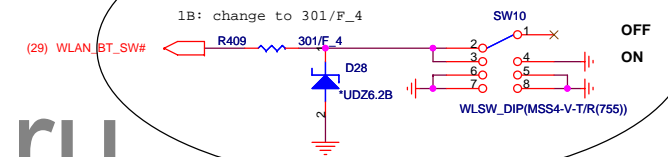
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



Win7 didn't support wake WLAN

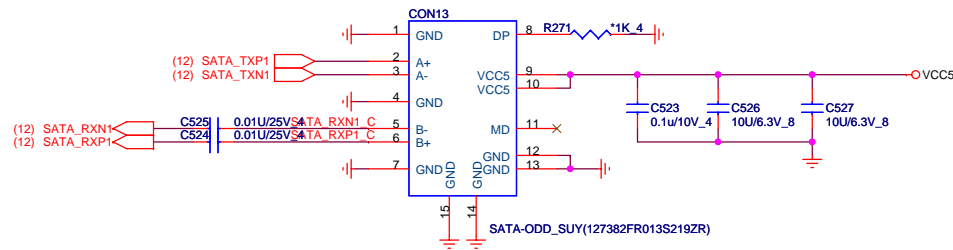
2A need check TOP or BOT again

WLAN_BT_SW

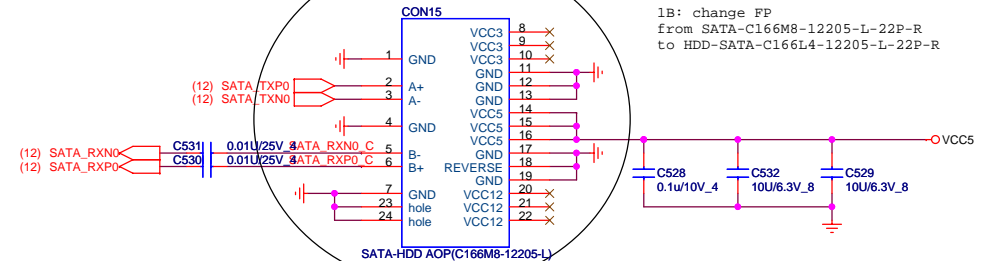


BTM Side , Right==>ON

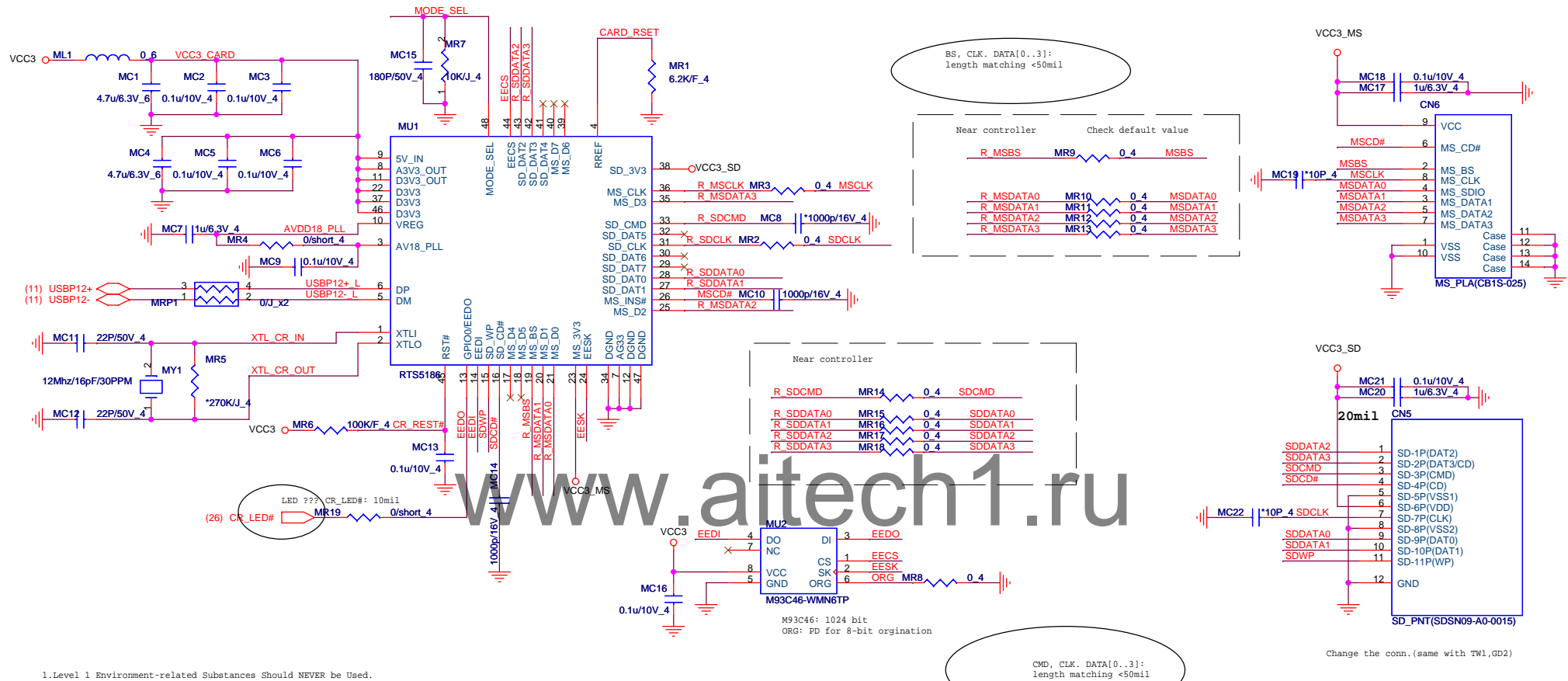
SATA ODD



2.5 inch SATA HDD

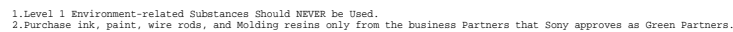


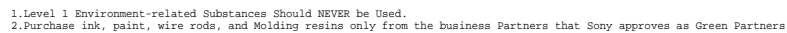
1B: change FP
from SATA-C166M8-12205-L-22P-R
to HDD-SATA-C166L4-12205-L-22P-R

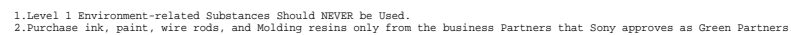


- 1.Level 1 Environment-related Substances Should NEVER be Used.
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2A : Remove Express card





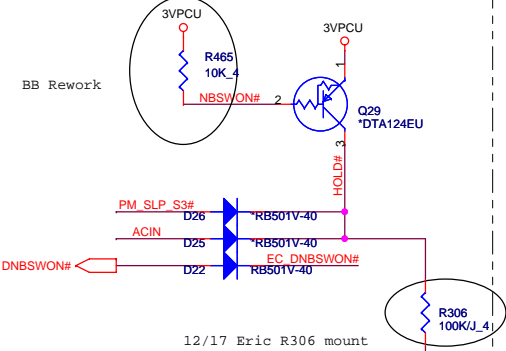


I/O Address		
BADDR1-0	Index	Data
1 0	2E	2F
1 1	4E	4F
0 0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1	
0 1	XOR-Tree TEST	

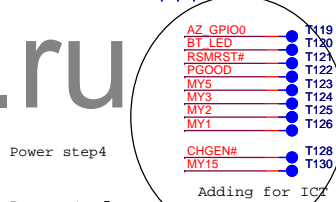
SHMB: SHMB(If = 0 Enable share host BIOS memory)

DOCK_RST# : BADDR0
T7: BADDR1

Reserved for more EC wake up function

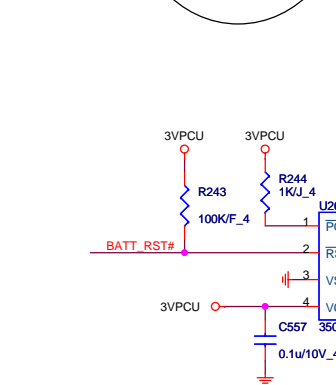


BATT_SCK R236 4.7K 4
BATT_SDA R307 4.7K 4
FUN_ASSIST# R304 10K 4



Power step4

Power step5

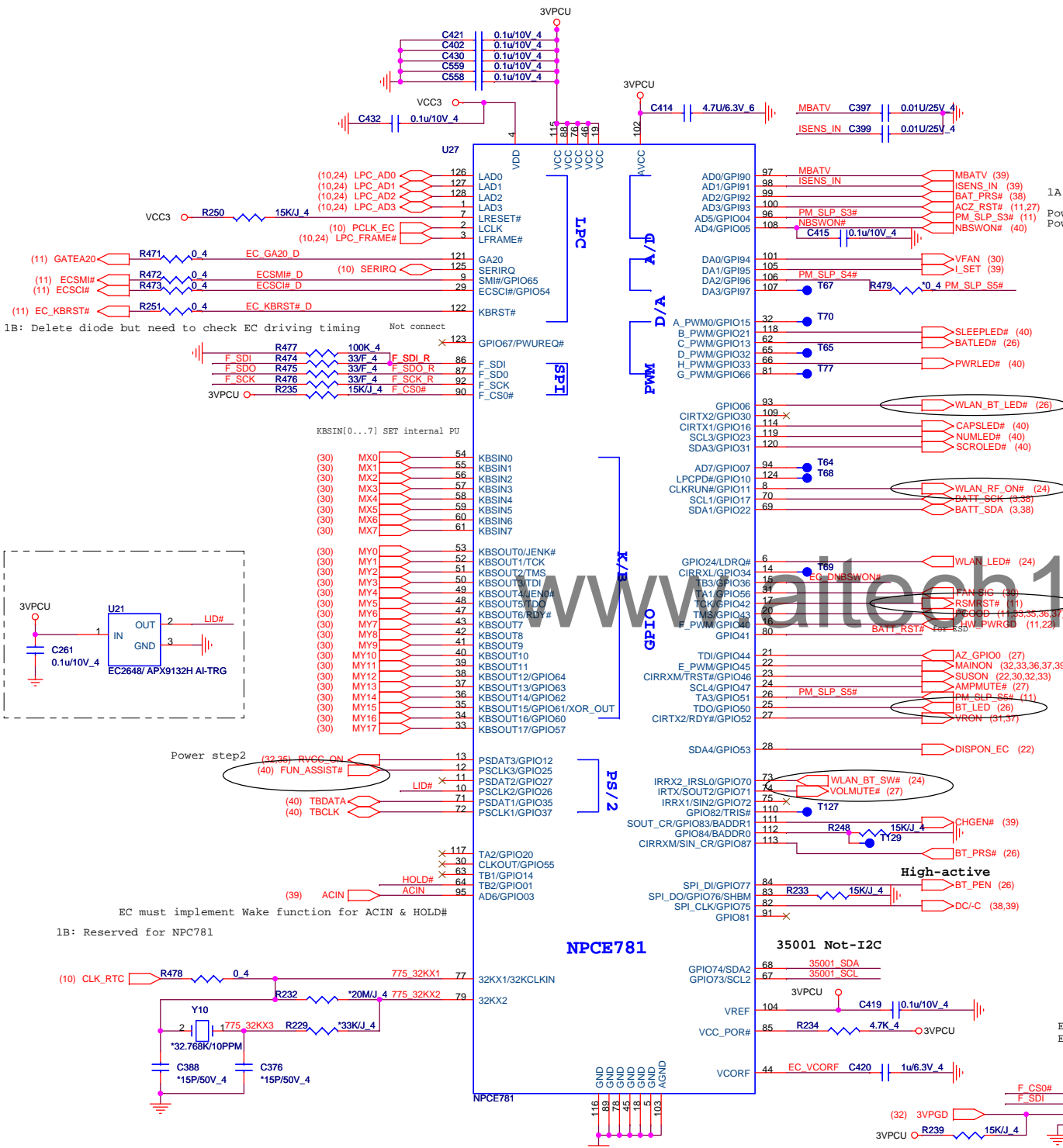


EC SDI-> EEPROM DO
EC SDO-> EEPROM DI



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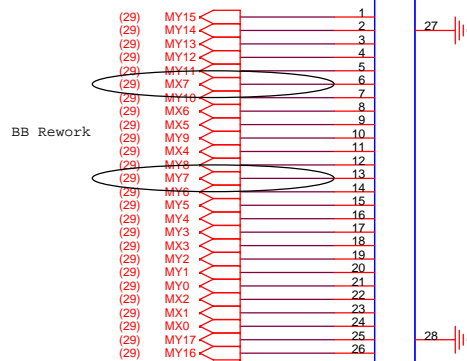
Size	Document Number	Rev
		2A
NPCE781 & FLASH		
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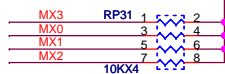
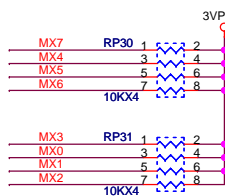
1. Level 1 Environment-related Substances should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

KEYBOARD

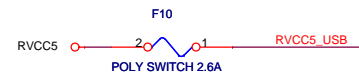
Matrix for working sample



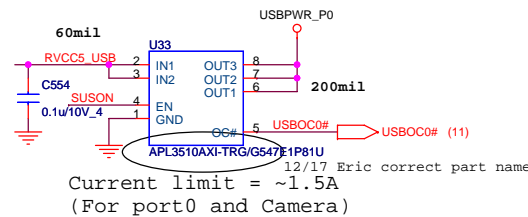
KB_ACS(88513-2641)



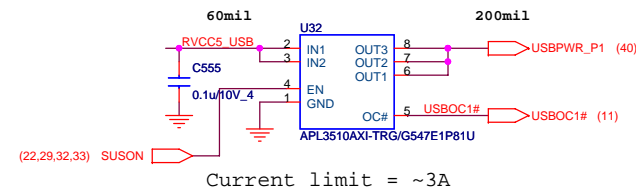
USB Port + e-SATA(USB)



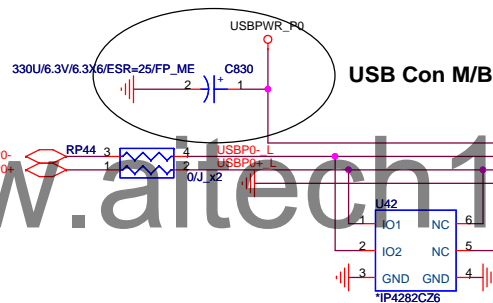
Current limit need to check



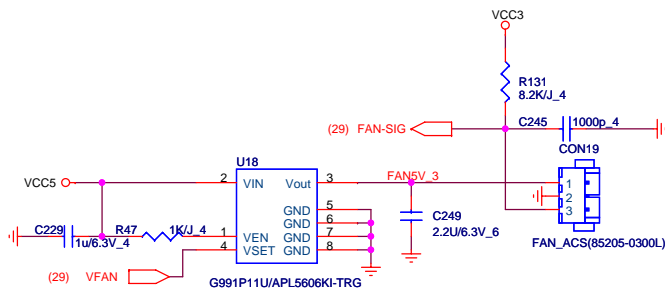
Current limit = ~1.5A
(For port0 and Camera)



Current limit = ~3A



FAN



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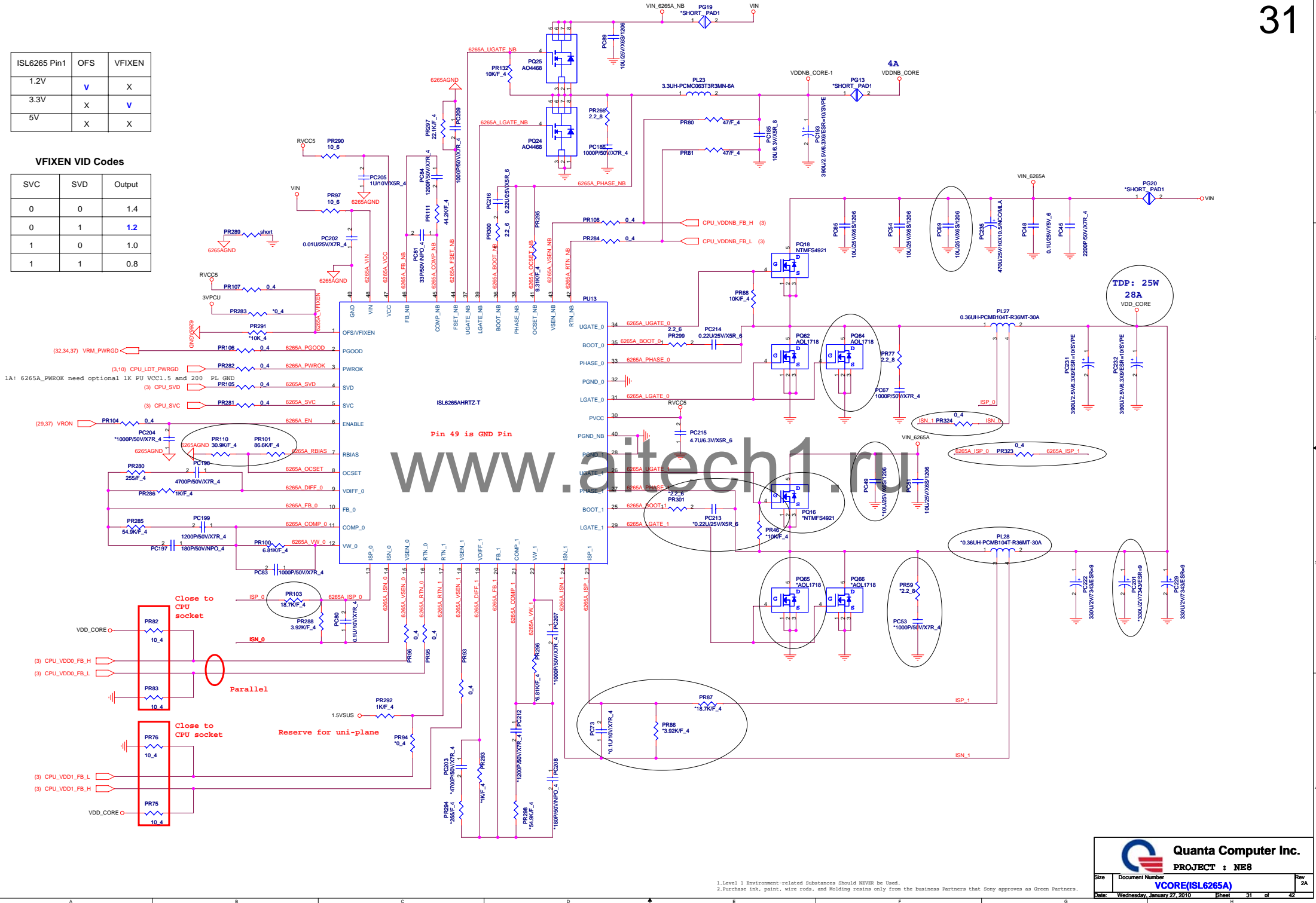
Quanta Computer Inc.
PROJECT : NE8

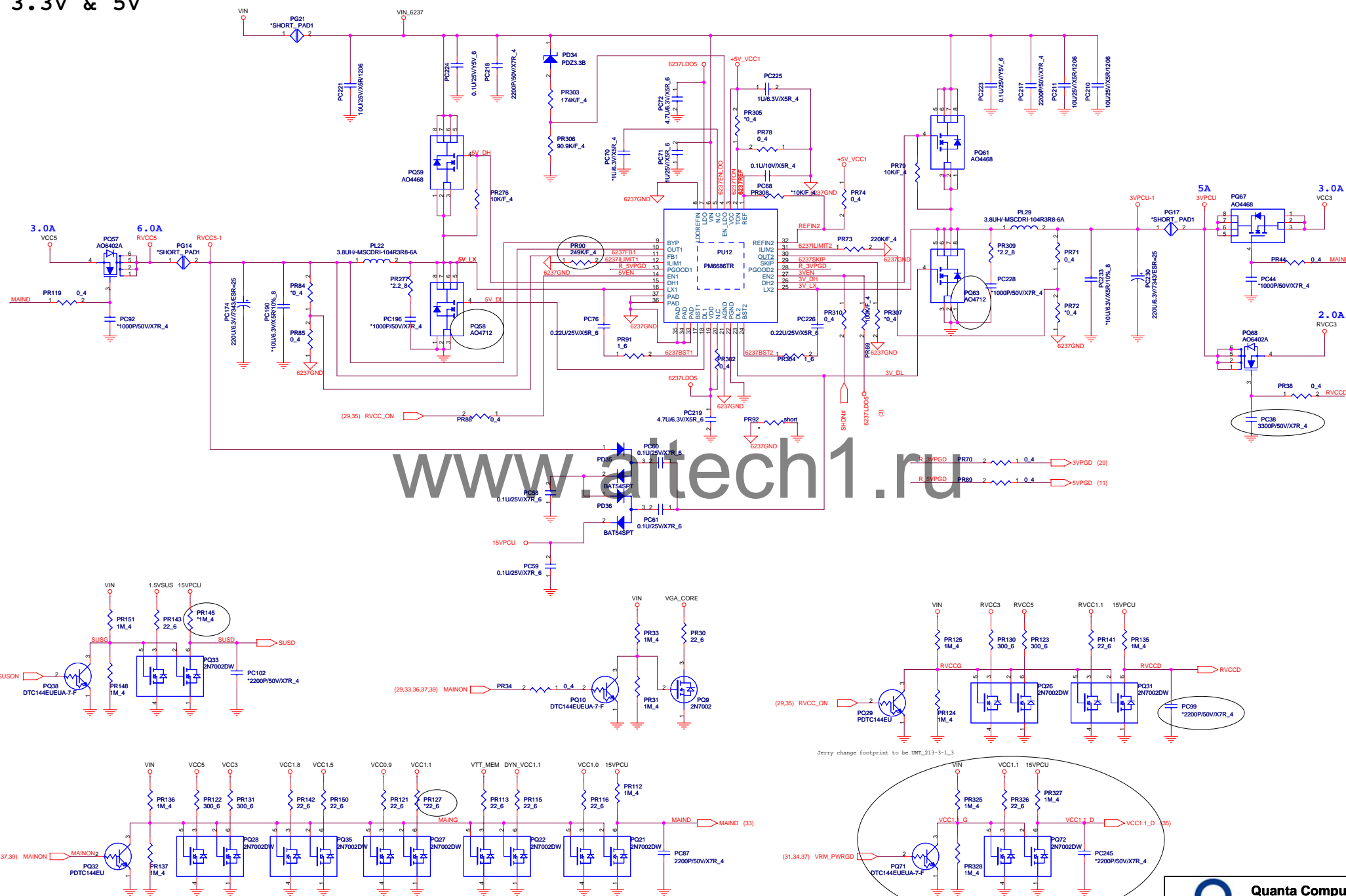
Size	Document Number	Rev
	KB/USB/FAN/PS	2A
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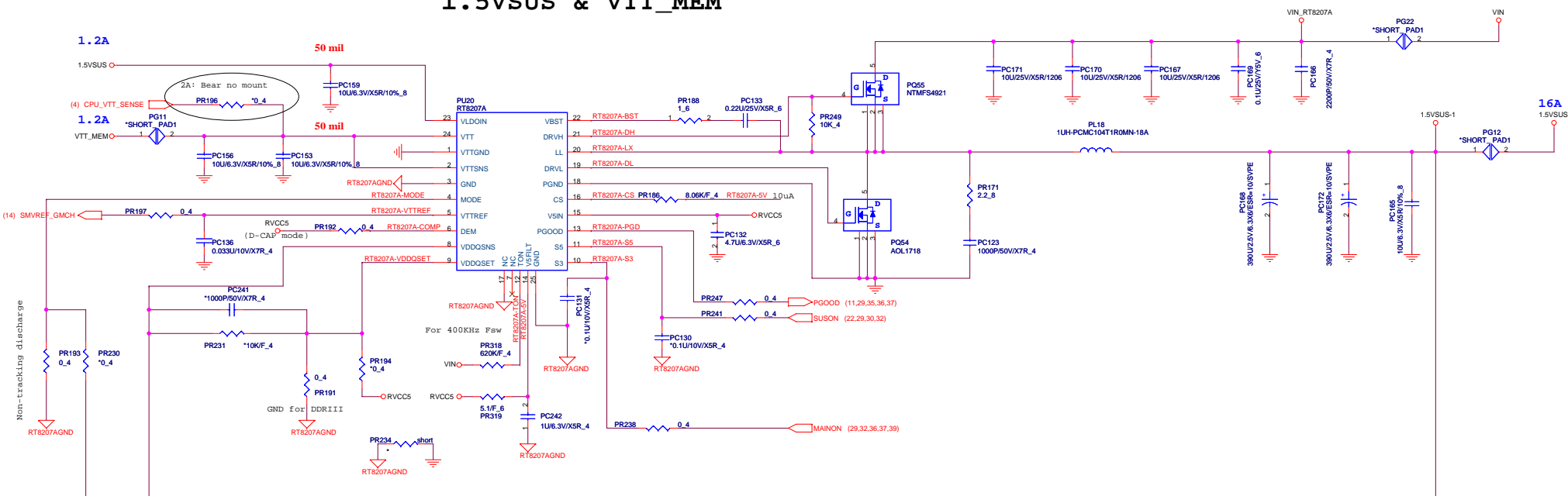
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

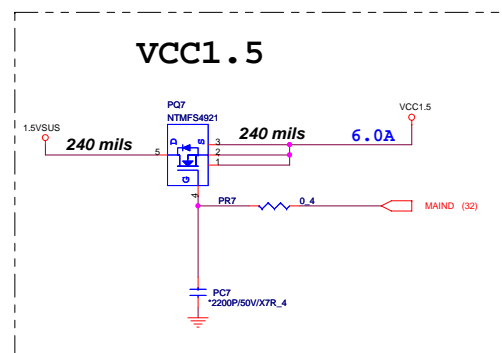
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





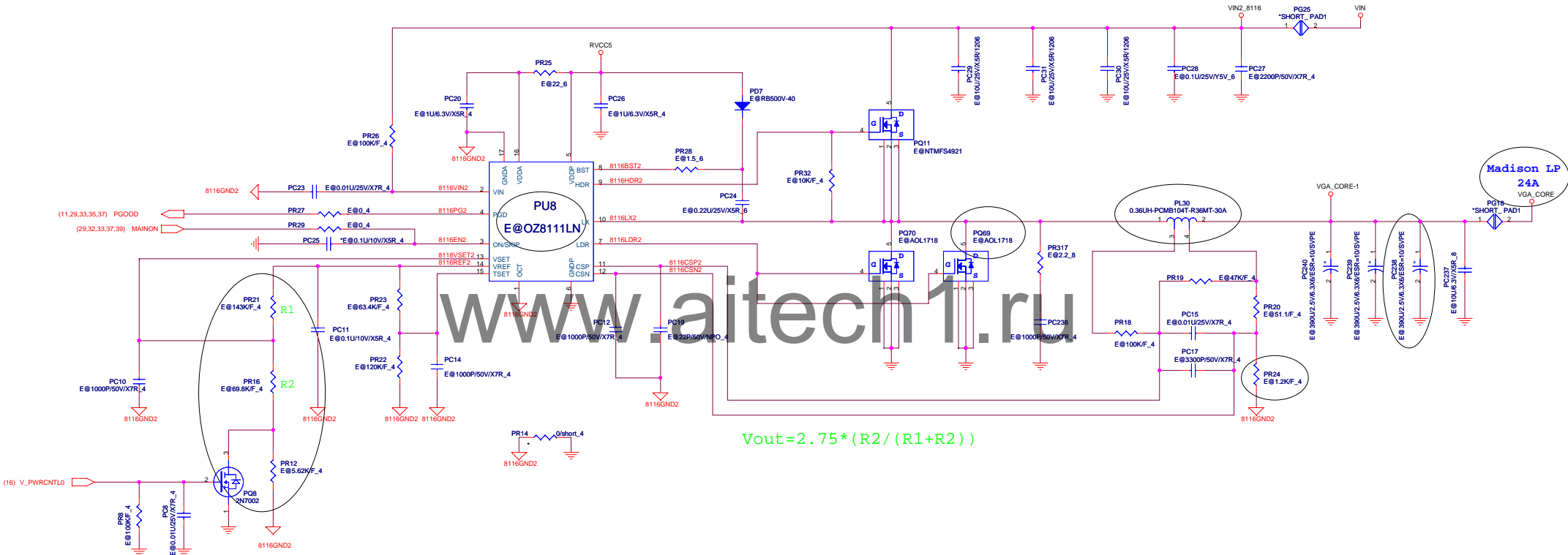


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VTT = VTTREF = VDDQSN5/2 = 0.75V

STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off



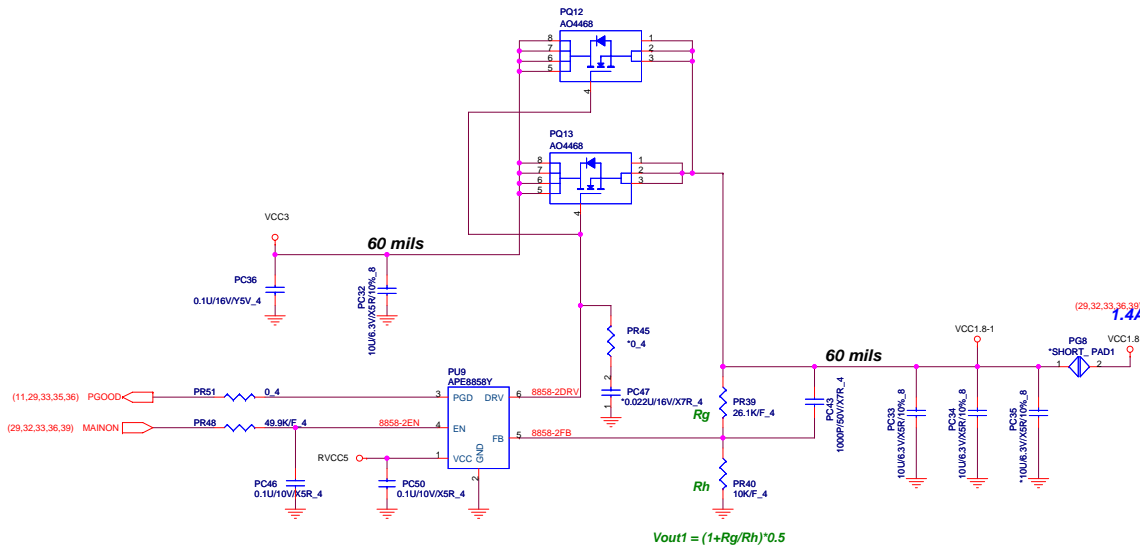
Madison LP

External VGA_CORE Voltage Setting:

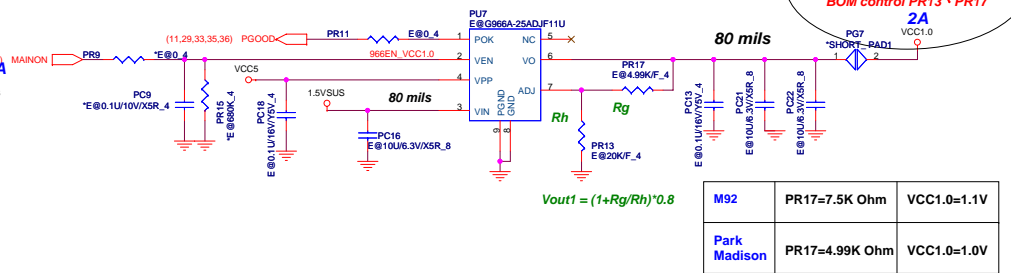
V_PWRCNTL0	VGA_CORE
0	0.95V
1	0.90V

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VCC1.8



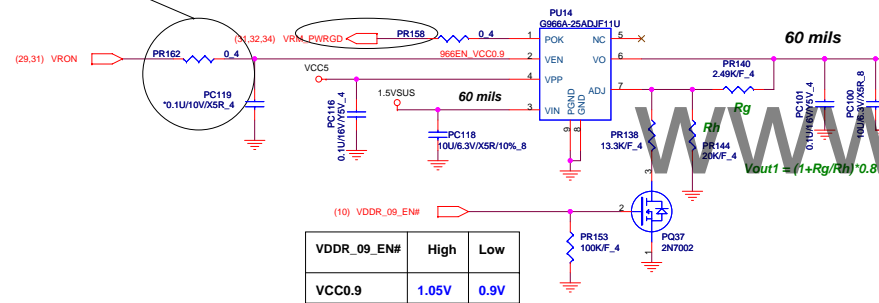
VCC1.0



NO change Vcc1.0 NET name
M9x : Vcc1.1
Manhattan : Vcc1.0
BOM control PR13 - PR17

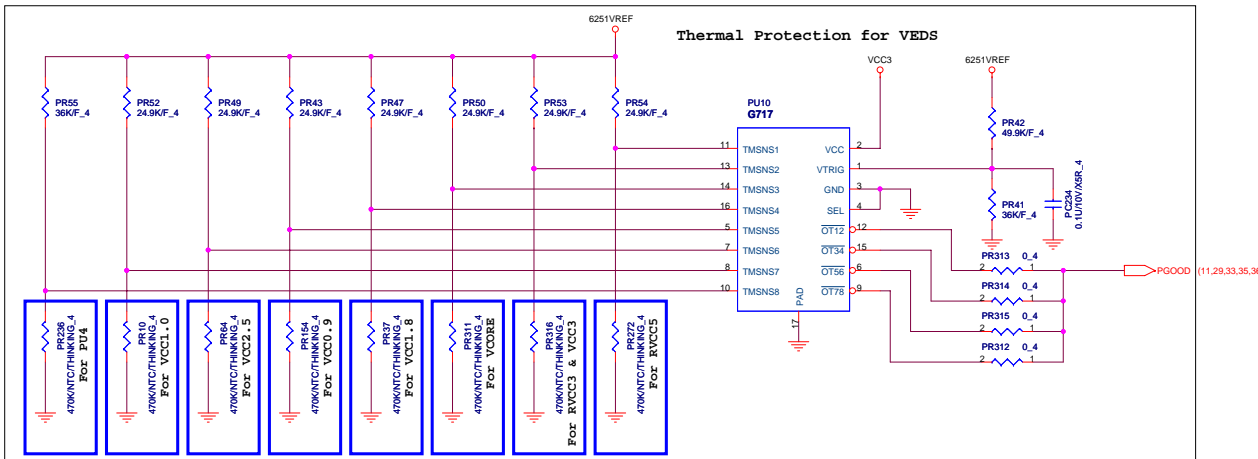
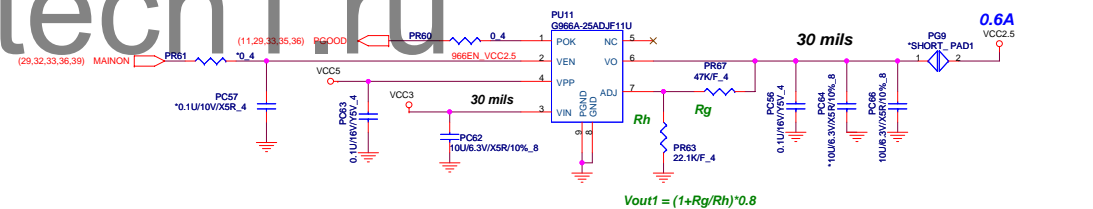
M92	PR17=7.5K Ohm	VCC1.0=1.1V
Park Madison	PR17=4.99K Ohm	VCC1.0=1.0V

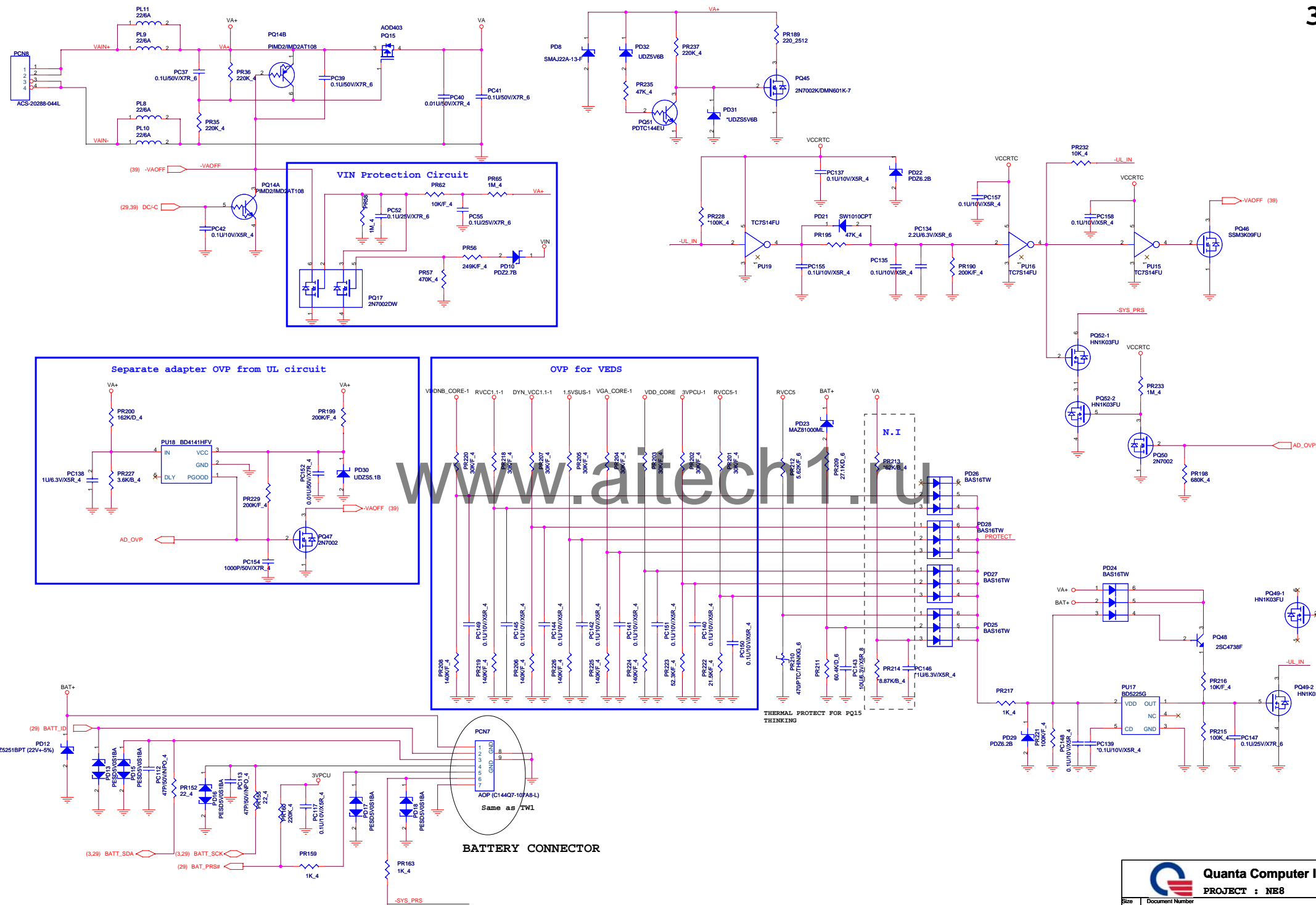
VCC0.9

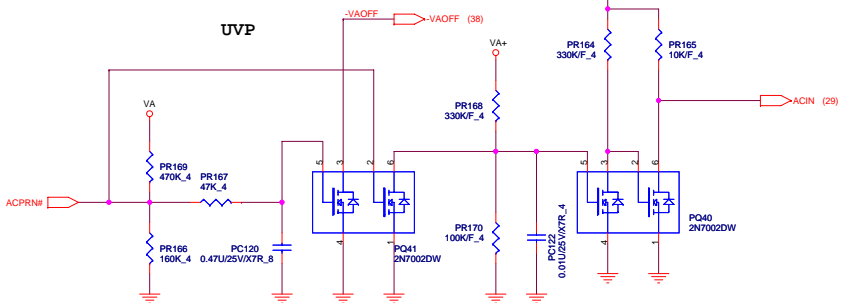


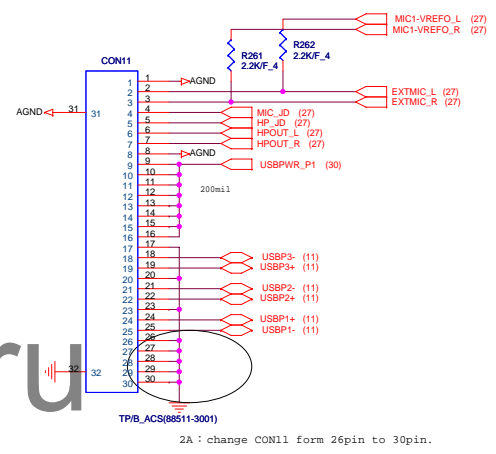
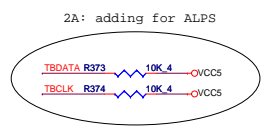
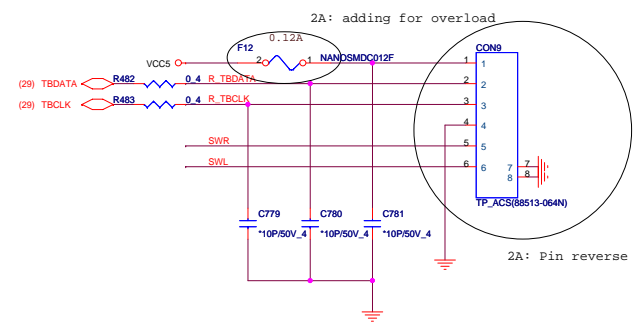
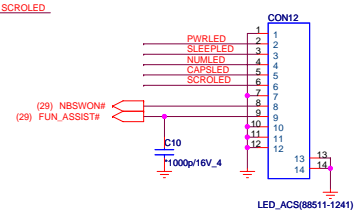
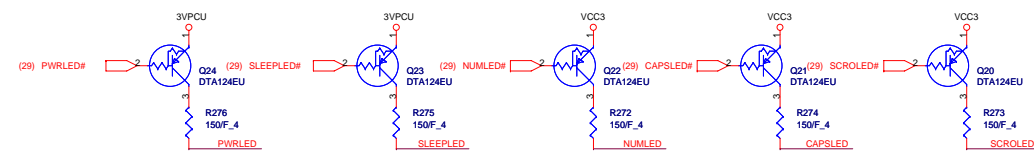
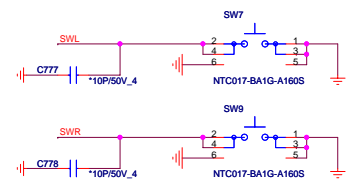
VDDR_09_EN#	High	Low
VCC0.9	1.05V	0.9V

VCC2.5

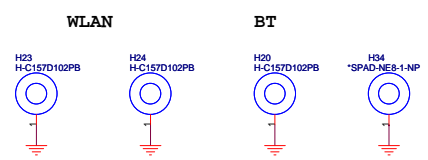
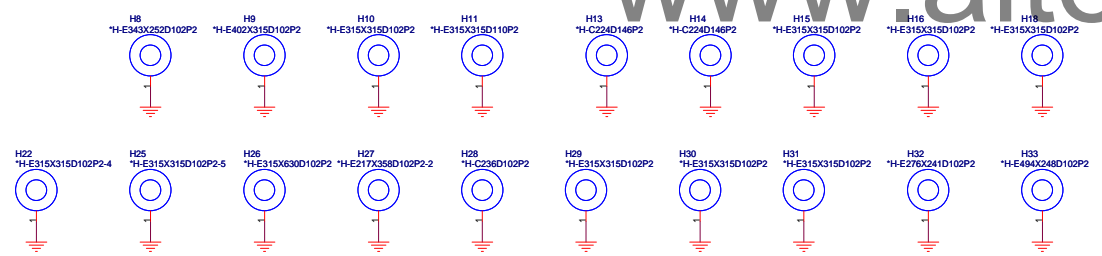








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Power on Sequence required:

- SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS
- RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3, +1.1V ramp before VCC_NB

CPU_LDT_RST#
(SB TO CPU)
CPU_LDT_PWRGD
(SB TO CPU)
CPU_CLKP/N

SB OUTPUT - - - -NB_PWRGD
SB INPUT - - - -SB_PWRGD

GROUP B
GROUP A

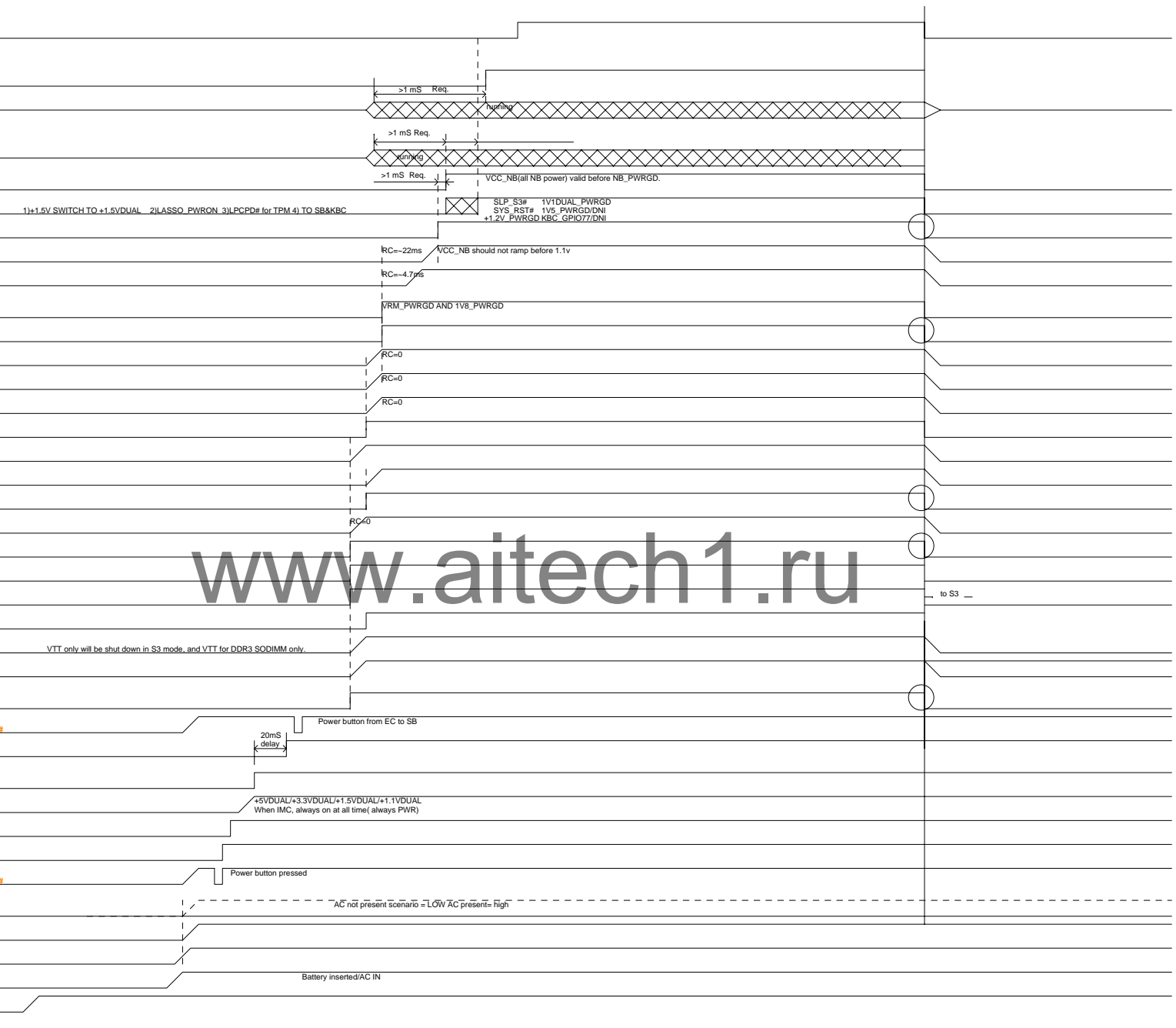
- PGOOD(DYN)
DYN_VCC1.1
VLDT(VCC1.1)
VCC1.1
VRM_PWRGD
VCC0.9
VDD_CORE (VRON)
VDDNB_CORE
PGOOD(2.5)
VCC2.5 (CPU_VDDA_2.5_RUN)
VCC1.5
PGOOD(1.8)
VCC1.8
VCC3, VCC5
MAINON
SUSON
PM_SLP_S3#
PGOOD(1.5)
MEM_VTT
1.5VSUS
PM_SLP_S5#
EC_DNBSWON#
RSMRST#
PGOOD(1.1)
RVCC5, RVCC3, RVCC1.1
VDD_DUAL_EN
RVCC_ON
EC_DNBSWON#
DNBSWON#
AC_OK (ACIN detect)
3VPCU
LDO:5.4V (from DCIN)
+VIN/+12V_HD
A_VBAT

CPU MEM CTL & DDR3 SODIMM PWRs

CPU_THM/SB/SB_SCL1/2
SB_XB/SPI/LPC ROM PWRs

KBC is ready

KBC is powered by A_VBAT & +3.3VALW



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1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

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